Keysight N6462A/N6462B DDR4 and LPDDR4 Compliance Test Application

KEYSIGHT TECHNOLOGIES

Methods of Implementation

Notices

Trademarks

UNIX is a registered trademark of UNIX System Laboratories in the U.S.A. and other countries. Target is copyrighted by Thru-Put Systems, Inc.

Manual Part Number

Version 01.15.0000 or greater

Edition

October 2015

Available in electronic format only

Keysight Technologies, Inc.
1900 Garden of the Gods Road
Colorado Springs, CO 80907 USA

Warranty

THE MATERIAL CONTAINED IN THIS DOCUMENT IS PROVIDED "AS IS," AND IS SUBJECT TO BEING CHANGED, WITHOUT NOTICE, IN FUTURE EDITIONS. FURTHER, TO THE MAXIMUM EXTENT PERMITTED BY APPLICABLE LAW, KEYSIGHT DISCLAIMS ALL WARRANTIES, EITHER EXPRESS OR IMPLIED WITH REGARD TO THIS MANUAL AND ANY INFORMATION CONTAINED HEREIN, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. KEYSIGHT SHALL NOT BE LIABLE FOR ERRORS OR FOR INCIDENTAL OR CONSEQUENTIAL DAMAGES IN CONNECTION WITH THE FURNISHING, USE, OR PERFORMANCE OF THIS DOCUMENT OR ANY INFORMATION CONTAINED HEREIN. SHOULD KEYSIGHT AND THE USER HAVE A SEPARATE WRITTEN AGREEMENT WITH WARRANTY TERMS COVERING THE MATERIAL IN THIS DOCUMENT THAT CONFLICT WITH THESE TERMS, THE WARRANTY TERMS IN THE SEPARATE AGREEMENT WILL CONTROL.

Technology Licenses

The hardware and/or software described in this document are furnished under a license and may be used or copied only in accordance with the terms of such license.

U.S. Government Rights

The Software is "commercial computer software," as defined by Federal Acquisition Regulation ("FAR") 2.101. Pursuant to FAR 12.212 and 27.405-3 and Department of Defense FAR Supplement ("DFARS") 227.7202, the U.S. government acquires commercial computer software under the same terms by which the software is customarily provided to the public. Accordingly, Keysight provides the Software to U.S. government customers under its standard commercial license, which is embodied in its End User License Agreement (EULA), a copy of which can be found at http://www.keysight.com/find/sweula. The license set forth in the EULA represents the exclusive authority by which the U.S. government may use, modify, distribute, or disclose the Software. The EULA and the license set forth therein, does not require or permit, among other things, that Keysight: (1) Furnish technical information related to commercial computer software or commercial computer software documentation that is not customarily provided to the public; or (2) Relinquish to, or otherwise provide, the government rights in excess of these rights customarily provided to the public to use, modify, reproduce, release, perform, display, or disclose commercial computer software or commercial computer software documentation. No additional government requirements beyond those set forth in the EULA shall apply, except to the extent that those terms, rights, or licenses are explicitly required from all providers of commercial computer software pursuant to the FAR and the DFARS and are set forth specifically in writing elsewhere in the EULA. Keysight shall be under no obligation to update, revise or otherwise modify the Software. With respect to any technical data as defined by FAR 2.101, pursuant to FAR 12.211 and 27.404.2 and DFARS 227.7102, the U.S. government acquires no greater than Limited Rights as defined in FAR 27.401 or DFAR 227.7103-5 (c), as applicable in any technical data.

Safety Notices

CAUTION

A CAUTION notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a CAUTION notice until the indicated conditions are fully understood and met.

WARNING

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

Terminology and Acronyms

The following terminology / acronyms have been used interchangeably in this document. There are:

DUT	Device Under Test
PUT	Pin Under Test
DDR4	Double Data Rate 4
LPDDR4	Low Power Double Data Rate 4
JEDEC	Joint Electronic Device Engineering Council
DRAM	Dynamic Random Access Memory
FBGA	Fine Ball Grid Array
SSTL	Stub Series Terminated Logic
OCD	Off-Chip Driver Impedance Adjustment
V_{TT}	Termination Voltage
V_{REF}	Reference Voltage
DQ	Data I/O
DQS	Data I/O Strobe
DIMM	Dual Inline Memory Module
ODT	On Die Termination

2.7 DDR4 SDRAM Addressing

2 Gb Addressing Table

Configuration		512 Mb x4	256 Mb x8	128 Mb x16
Bank Address	# of Bank Groups	4	4	2
	BG Address	BG0~BG1	BG0~BG1	BG0
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
Row Address		A0~A14	A0~A13	A0~A13
Column Address		A0~A9	A0~A9	A0~A9
Page size		512B	1KB	2KB

4 Gb Addressing Table

Configuration		1 Gb x4	512 Mb x8	256 Mb x16
Bank Address	# of Bank Groups	4	4	2
	BG Address	BG0~BG1	BG0~BG1	BG0
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
Row Address		A0~A15	A0~A14	A0~A14
Column Address		A0~A9	A0~A9	A0~A9
Page size		512B	1KB	2KB

8 Gb Addressing Table

Configuration		2 Gb x4	1 Gb x8	512 Mb x16
Bank Address	# of Bank Groups	4	4	2
	BG Address	BG0~BG1	BG0~BG1	BG0
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
Row Address		A0~A16	A0~A15	A0~A15
Column Address		A0~A9	A0~A9	A0~A9
Page size		512B	1KB	2KB

16 Gb Addressing Table

Configuration		4 Gb x4	2 Gb x8	1 Gb x16
Bank Address	# of Bank Groups	4	4	2
	BG Address	BG0~BG1	BG0~BG1	BG0
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
Row Address		A0~A17	A0~A16	A0~A16
Column Address		A0~A9	A0~A9	A0~A9
Page size		512B	1KB	2KB

Figure 1 Available Pin-Out/Signals on DDR4 DIMM

Typical LPDDR4 Signals Reference

3.1 LPDDR4 SDRAM Addressing

Table 2 — LPDDR4 SDRAM Addressing

Memory Density (per Die)	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb
Memory Density (per channel)	2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb
Configuration	16Mb x 16DQ x 8 banks x 2 channels	24Mb x 16DQ x 8 banks x 2 channels	32Mb x 16DQ x 8 banks x 2 channels	48Mb x 16DQ x 8 banks x 2 channels	64Mb x 16DQ x 8 banks x 2 channels	TBD x 16DQ x TBD banks x 2 channels	TBD x 16DQ x TBD banks x 2 channels
Number of Channels (per die)	2	2	2	2	2	2	2
Number of Banks (per channel)	8	8	8	8	8	TBD	TBD
Array Pre-Fetch (bits, per channel)	256	256	256	256	256	256	256
Number of Rows (per channel)	16,384	24,576	32,768	49,152	65,536	TBD	TBD
Number of Columns (fetch boundaries)	64	64	64	64	64	TBD	TBD
Page Size (Bytes)	2048	2048	2048	2048	2048	TBD	TBD
Channel Density (Bits per channel)	2,147,483,648	3,221,225,472	4,294,967,296	6,442,450,944	8,589,934,592	12,884,901,888	17,179,869,184
Total Density (Bits per die)	4,294,967,296	6,442,450,944	8,589,934,592	12,884,901,888	17,179,869,184	25,769,803,776	34,359,738,368
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2	BA0 - BA2	BA0 - BA2	TBD	TBD
x16 Row Addresses	R0 - R13	R0 - R14 (R13=0 when R14=1)	R0 - R14	R0 - R15 (R14=0 when R15=1)	R0 - R15	TBD	TBD
x16 Column Addresses	C0 - C9	C0 - C9	C0 - C9	C0 - C9	C0 - C9	TBD	TBD
Burst Starting Address Boundary	64 - bit	64 - bit	64 - bit	64 - bit	64 - bit	64 - Bit	64 - bit

NOTE 1 The lower two column addresses (C0 - C1) are assumed to be "zero" and are not transmitted on the CA bus.

NOTE 2 Row and Column address values on the CA bus that are not used for a particular density be at valid logic levels.

NOTE 3 For non - binary memory densities,only half of the row address space is valid. When the MSB address bit is "HIGH", then the MSB - 1 address bit must be "LOW".

NOTE 4 TBD, as of publication of this document, under discussion by the formulating committee.

Figure 2 Available Pin-Out/Signals on LPDDR4 DIMM

Contents

1 Requirements for Testing

KEYSIGHT TECHNOLOGIES

Hardware Required for Testing

Common hardware requirements:

- Ocsillocope: 9000A Series, 90000A Series, 90000 X-Series, 90000 Q-Series, and Z-Series:
  - Minimum 8 GHz bandwidth is recommended to get accurate measurements.
  - 13 GHz bandwidth is recommended to get accurate measurements for faster speed grade devices.
- Any PC motherboard system that support DDR4 memory DIMM(s)
- DUT: Saved waveform and PulseGen generated signal
- InfiniiMax probe amplifiers:
  - 1169A – 12 GHz InfiniiMax II probe amplifier
  - N2803A – 30 GHz InfiniiMax III probe amplifier
  - N2802A – 25 GHz InfiniiMax III probe amplifier
  - N2801A – 20 GHz InfiniiMax III probe amplifier
  - N2800A – 16 GHz InfiniiMax III probe amplifier
  - N2831A – 8 GHz InfiniiMax III probe amplifier
  - N2832A – 12 GHz InfiniiMax III probe amplifier
- InfiniiMax probe heads – InfiniiMax I/II probe heads and accessories (compatible with 9000 Series and 90000 Series, use N5442A precision BNC adapter with 90000X/Q Series):
  - N5381A – InfiniiMax II 12 GHz differential solder-in probe head and accessories
  - N5382A – InfiniiMax II 12 GHz differential browser
  - E2677A – InfiniiMax II 12 GHz differential solder-in probe head and accessories
  - N5425A – InfiniiMax II 12 GHz ZIF probe head
  - N5426A – InfiniiMax II ZIF tips (×10)
- InfiniiMax III probe heads and accessories:
  - N5451A – Long Wire tips (×10)
  - N5439A – ZIF probe head
  - N5445A – Browser (hand held) probe head
  - N5441A – Solder-in probe head
  - N2838A - 450 Ω PCB ZIF tips (set of 5)
  - N2848A – InfiniiMax III QuickTip head
  - N2849A – InfiniiMax III Quick tips (4 per kit)

Software Required for Testing

Installed on the oscilloscope:

- Infiniium baseline software
- Keysight N6462A/N6462B DDR4 and LPDDR4 compliance test application
- Keysight E2688A Serial Data Analysis (SDA) software

Other software:

- N/A

Option Licenses Required for Testing

Required licenses:

- N6462A/N6462B DDR4 compliance test application (DD4).
- N6462A/N6462B LPDDR4 compliance test application (LP4).
- E2688A High-speed serial data analysis/mask testing with clock recovery (SDA).
- N5414A InfiniiScan event identification software (SWT).

2 Installing the DDR4 and LPDDR4 Compliance Test Application

If you purchased the N6462A/N6462B DDR4 and LPDDR4 Compliance Test Application separate from your Infiniium oscilloscope, you need to install the software and license key.

KEYSIGHT TECHNOLOGIES

Installing the Software

1 Make sure you have the minimum version of Infiniium oscilloscope software (see the N6462A/N6462B release notes) by choosing **Help > About Infiniium...** from the main menu.
2 To obtain the DDR4 and LPDDR4 Compliance Test Application, go to Keysight website: "http://www.keysight.com/find/N6462A"
3 In the web page's **Trials & Licenses** tab, there is a button for downloading software; click it, and follow the instructions to download and install the application software.

Installing the License Key

1 Request a license code from Keysight by following the instructions on the Entitlement Certificate.

   You will need the oscilloscope's "Option ID Number", which you can find in the **Help > About Infiniium...** dialog box.

2 After you receive your license code from Keysight, choose **Utilities > Install Legacy Licenses...**.

3 In the Install Option License dialog, enter your license code and click **Install License**.

4 Click **OK** in the dialog that tells you to restart the Infiniium oscilloscope application software to complete the license installation.

5 Click **Close** to close the Install Option License dialog.

6 Choose **File > Exit**.

7 Restart the Infiniium oscilloscope application software to complete the license installation.

3 Preparing to Take Measurements

Before running the DDR4/LPDDR4 automated tests, you should calibrate the oscilloscope and probe. No test fixture is required for this application. After the oscilloscope and probe have been calibrated, you are ready to start the DDR4 and LPDDR4 Compliance Test Application and perform the measurements.

Calibrating the Oscilloscope

If you haven't already calibrated the oscilloscope, see Appendix B, “Calibrating the Infiniium Oscilloscope and Probe,” starting on page 195.

NOTE

If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities > Calibration** menu.

NOTE

If you switch cables between channels or other oscilloscopes, it is necessary to perform cable and probe calibration again. Keysight recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the DDR4 and LPDDR4 Compliance Test Application

1 Ensure that the DDR4 Device Under Test (DUT) is operating and set to desired test modes.

2 To start the DDR4 and LPDDR4 Compliance Test Application: From the Infiniium oscilloscope's main menu, choose **Analyze > Automated Test Apps > N6462A/N6462B DDR4 Test App**.

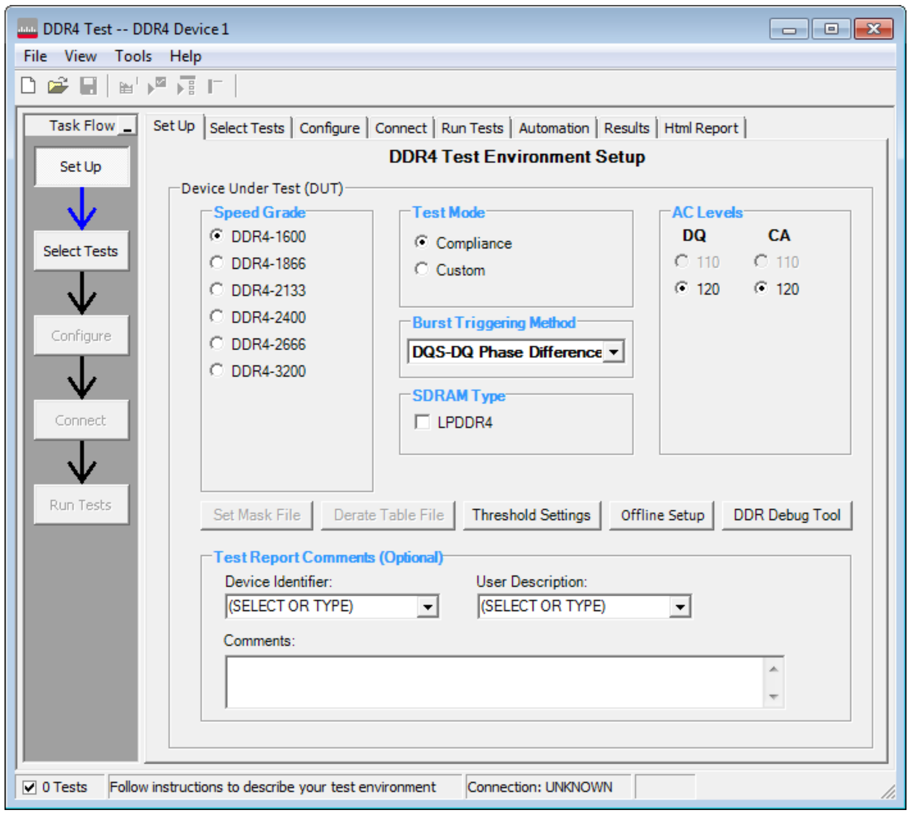


Figure 3 DDR4 and LPDDR4 Compliance Test Application Main Window

The task flow pane, and the tabs in the main pane, show the steps you take in running the automated tests:

Set Up	Lets you identify and set up the test environment, including information about the device under test. The **Device Identifier**, **User Description**, and **Comments** are all printed in the final HTML report.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure test parameters (for example, channels used in test, voltage levels, etc.).
Connect	Shows you how to connect the oscilloscope to the device under test for the tests that are to be run.
Run Tests	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Automation	Lets you construct scripts of commands that drive execution of the application.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

4 Electrical Tests Group

Overview

The following group of tests pertains to the electrical AC operating conditions of a DDR4 or LPDDR4 DRAM as defined in JEDEC specification. The tests are further divided into Single-Ended Signals Tests and Differential Signals Tests.

Single-Ended Signals Tests

V_{IH} Test – Input Logic High

V_{IH} Test can be divided into 4 sub tests: $V_{IH.CA\ (AC)}$, $V_{IH.DQ\ (AC)}$, $V_{IH.CA\ (DC)}$, and $V_{IH.CA\ (DC)}$.

$V_{IH.CA\ (AC)}$ Test – AC Input Logic High for Command and Address

Mode Supported: DDR4

Signal cycle of interest: READ or WRITE

Require Read/Write separation: No

Signal(s) of Interest:

- Address Signals OR
- Control Signals

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the high level voltage value of the test signal within a valid sampling window. The limit is definable by the customers for their evaluation tests usage.

Procedure:

1. Sample/acquire signal data.
2. Find all valid positive pulses. A valid positive pulse starts at V_{REF} crossing at valid rising edge and end at V_{REF} crossing at the following valid falling edge (See notes on "Threshold Settings" on page 69).
3. Zoom in on the first valid positive pulse and perform V_{TOP} measurement. Take the V_{TOP} measurement results as $V_{IH.CA\ (AC)}$ value.
4. Continue the previous step with another 9 valid positive pulses that were found in the burst.
5. Determine the worst result from the set of $V_{IH.CA\ (AC)}$ measured.

Expected/Observable Results: The high level voltage value of the test signal shall meet the user defined limit.

$V_{IH.CA\ (DC)}$ Test – DC Input Logic High for Command and Address

Mode Supported: DDR4

Signal cycle of interest: READ or WRITE

Require Read/Write separation: No

Signal(s) of Interest:
- Address Signals OR
- Control Signals

Required Signals: Needed to perform this test on oscilloscope:
- Pin Under Test, PUT = any of the signal of interest defined above.

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the histogram mode value of the test signal within a valid sampling window. The limit is definable by the customers for their evaluation tests usage.

Procedure:
1. Sample/acquire signal data.
2. Find all valid positive pulses. A valid positive pulse starts at V_{REF} crossing at valid rising edge and end at V_{REF} crossing at the following valid falling edge (See notes on "Threshold Settings" on page 69).
3. Zoom in on the first valid positive pulse and perform V_{TOP} measurement. Take the V_{TOP} measurement results as $V_{IH.CA\ (DC)}$ value.
4. Continue the previous step with another 9 valid positive pulses that were found in the burst.
5. Determine the worst result from the set of $V_{IH.CA\ (DC)}$ measured.

Expected/Observable Results: The high level voltage value of the test signal shall meet the user defined limit.

V_{IL} Test – AC Input Logic Low

V_{IL} Test can be divided into 4 sub tests: $V_{IL.CA\ (AC)}$, $V_{IL.DQ\ (AC)}$, $V_{IL.CA\ (DC)}$, and $V_{IL.DQ\ (DC)}$.

$V_{IL.CA\ (AC)}$ Test – AC Input Logic Low for Command and Address

Mode Supported: DDR4

Signal cycle of interest: READ or WRITE

Require Read/Write separation: No

Signal(s) of Interest:
- Address Signals OR
- Control Signals

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the low level voltage value of the test signal within a valid sampling window. The limit is definable by the customers for their evaluation tests usage.

Procedure:

1. Sample/acquire signal data.
2. Find all valid negative pulses. A valid negative pulse starts at V_{REF} crossing at valid falling edge and end at V_{REF} crossing at the following rising valid edge (See notes on "Threshold Settings" on page 69).
3. Zoom in on the first valid negative pulse and perform V_{BASE} measurement. Take the V_{BASE} measurement results as $V_{IL.CA\ (AC)}$ value.
4. Continue the previous step with another 9 valid negative pulses.
5. Determine the worst result from the set of $V_{IL.CA\ (AC)}$ measured.

Expected/Observable Results: The histogram mode value of the test signal shall meet the user defined limit.

$V_{IL.CA\ (DC)}$ Test – DC Input Logic Low for Command and Address

Mode Supported: DDR4

Signal cycle of interest: READ or WRITE

Require Read/Write separation: No

Signal(s) of Interest:

- Address Signals OR
- Control Signals

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the histogram mode value of the test signal within a valid sampling window. The limit is definable by the customers for their evaluation tests usage.

Procedure:

1. Sample/acquire signal data.
2. Find all valid negative pulses. A valid negative pulse starts at V_{REF} crossing at valid falling edge and end at V_{REF} crossing at the following rising valid edge (See notes on "Threshold Settings" on page 69).
3. Zoom in on the first valid negative pulse and perform V_{BASE} measurement. Take the V_{BASE} measurement results as $V_{IL.CA\ (DC)}$ value.
4. Continue the previous step with another 9 valid negative pulses.

5 Determine the worst result from the set of $V_{IL.CA\ (DC)}$ measured.

Expected/Observable Results: The low level voltage value of the test signal shall meet the user defined limit.

Single-Ended Levels for Strobes

Single-Ended Levels for Strobe can be divided into 2 sub tests: V_{SEH} test and V_{SEL}.

V_{SEH} – Single-ended High Level

Mode Supported: DDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signals (supported by Data Signals)

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin = DQ

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the maximum voltage of high pulse. The limit is definable by the customers for their evaluation tests usage.

Procedure:

1 Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)
2 Take the first valid WRITE burst found.
3 Find all valid Strobe positive pulse in the said burst. A valid Strobe positive pulse starts at V_{REF} crossing at valid Strobe rising edge and end at V_{REF} crossing at following valid Strobe falling edge (See notes on "Threshold Settings" on page 69).
4 Zoom into the first pulse and perform T_{MAX}. Perform V_{TIME} with the found T_{MAX} to obtain the maximum voltage of the pulse. Take the V_{TIME} measurement as V_{SEH} value.
5 Continue previous step with the rest of the positive pulses in the said burst.
6 Determine the worst result from the set of V_{SEH} measured.

Expected/Observable Results: The worst measured V_{SEH} shall meet the user defined limit.

V_{SEL} – Single-ended Low Level

Mode Supported: DDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signals (supported by Data Signals)

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin = DQ

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the minimum voltage of low pulse. The limit is definable by the customers for their evaluation tests usage.

Procedure:

1. Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)
2. Take the first valid WRITE burst found.
3. Find all valid Strobe negative pulse in the said burst. A valid Strobe negative pulse starts at V_{REF} crossing at valid Strobe falling edge and end at V_{REF} crossing at following valid Strobe rising edge (See notes on "Threshold Settings" on page 69).
4. Zoom into the first pulse and perform T_{MIN}. Perform V_{TIME} with the found T_{MIN} to obtain the minimum voltage of the pulse. Take the V_{TIME} measurement as V_{SEL} value.
5. Continue previous step with the rest of the negative pulses in the said burst.
6. Determine the worst result from the set of V_{SEL} measured.

Expected/Observable Results: The worst measured V_{SEL} shall meet the user defined limit.

Single-Ended Levels for Clocks

Single-Ended Levels for Strobe can be divided into 2 sub tests: V_{SEH} test and V_{SEL}.

V_{SEH} – Single-ended High Levels

Mode Supported: DDR4

Signal cycle of interest: READ or WRITE

Require Read/Write separation: No

Signal(s) of Interest:
- Clock Signals

Required Signals: Needed to perform this test on oscilloscope:
- Pin Under Test, PUT = any of the signal of interest defined above.

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the maximum voltage of high pulse. The limit is definable by the customers for their evaluation tests usage.

Procedure:
1. Pre-condition the oscilloscope.
2. Trigger on the rising edge of the clock signal under test.
3. Find all valid Clock positive pulse in the entire waveform. A valid Clock positive pulse starts at V_{REF} crossing at valid Clock rising edge and end at V_{REF} crossing at following valid Clock falling edge (See notes on "Threshold Settings" on page 69).
4. Zoom into the first pulse and perform T_{MAX}. Perform V_{TIME} with the found T_{MAX} to obtain the maximum voltage of the pulse. Take the V_{TIME} measurement as V_{SEH} value.
5. Continue the previous step with another 9 valid positive pulses found in the said waveform.
6. Determine the worst result from the set of V_{SEH} measured.

Expected/Observable Results: The worst measured V_{SEH} shall meet the user defined limit.

V_{SEL} – Single-ended Low Level

Mode Supported: DDR4

Signal cycle of interest: READ or WRITE

Require Read/Write separation: No

Signal(s) of Interest:
- Clock Signals

Required Signals: Needed to perform this test on oscilloscope:
- Pin Under Test, PUT = any of the signal of interest defined above.

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the minimum voltage of low pulse. The limit is definable by the customers for their evaluation tests usage.

Procedure:

1. Pre-condition the oscilloscope.
2. Triggered on falling edge of the clock signal under test.
3. Find all valid Clock negative pulse in the entire waveform. A valid Clock negative pulse starts at V_{REF} crossing at valid Clock falling edge and end at V_{REF} crossing at following valid Clock rising edge (See notes on "Threshold Settings" on page 69).
4. Zoom into the first pulse and perform T_{MIN}. Perform V_{TIME} with the found T_{MIN} to obtain the minimum voltage of the pulse. Take the V_{TIME} measurement as V_{SEL} value.
5. Continue the previous step with another 9 valid negative pulses found in the said waveform.
6. Determine the worst result from the set of V_{SEL} measured.

Expected/Observable Results: The worst measured V_{SEL} shall meet the user defined limit.

V_{OH} Test – Output Logic High

V_{OH} Test can be divided into 2 sub tests: $V_{OH\ (AC)}$ test and $V_{OH\ (DC)}$.

$V_{OH\ (AC)}$ Test – AC Output Logic High

Mode Supported: DDR4 , LPDDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signals (supported by Data Strobe Signals) OR
- Data Strobe Signals (supported by Data Signals) OR

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin is DQS or DQ depend on the PUT selected.

References:

Specifications document	Section#	Table#
DDR4 SDRAM Specification, JESD79-4, September 2012	8	Table 74
LPDDR4 SDRAM Specification, JESD209-4, August 2014	7.1.3.2	Table 69

Table 74 — Single-ended AC & DC output levels

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/3200	Units	NOTE
$V_{OH}(AC)$	AC output high measurement level (for output SR)	$(0.7 + 0.15) \times V_{DDQ}$	V	1

Table 69 — Single-ended AC and DC Output Levels

Parameter	Symbol	Min	Max	Unit
Output high voltage	VOH	$0.80 * V_{DD}Q$	-	V
Output low voltage	VOL	-	$0.20 * V_{DD}Q$	V

Test Overview: The purpose of this test is to verify that the high level voltage value of the test signal within a valid sampling window is greater than the conformance limits of the $V_{OH\ (AC)}$ value specified in the JEDEC specification.

Procedure:

1. Acquire and split read and write burst of the acquired signal.
2. Take the first valid READ burst found.
3. Find all valid positive pulses in the said burst. A valid positive pulse starts at V_{REF} crossing at valid rising edge and end at V_{REF} crossing at the following valid falling edge (See notes on "Threshold Settings" on page 69).
4. Zoom in on the first valid positive pulse and perform V_{TOP} measurement. Take the V_{TOP} measurement results as $V_{OH\ (AC)}$ value.
5. Continue the previous step with the rest of the valid positive pulses that were found in the burst.
6. Determine the worst result from the set of $V_{OH\ (AC)}$ measured.

Expected/Observable Results: The high level voltage value of the test signal shall be greater than or equal to the $V_{OH\ (AC)}$ value in the specification.

$V_{OH\ (DC)}$ Test – DC Output Logic High

Mode Supported: DDR4, LPDDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signals (supported by Data Strobe Signals) OR
- Data Strobe Signals (supported by Data Signals)

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin is DQS or DQ depend on the PUT selected.

References:

Specifications document	Section#	Table#
DDR4 SDRAM Specification, JESD79-4, September 2012	8	Table 74

Table 74 — Single-ended AC & DC output levels

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/3200	Units	NOTE
V_{OH}(DC)	DC output high measurement level (for IV curve linearity)	1.1 x V_{DDQ}	V	

Test Overview: The purpose of this test is to verify that the high level voltage valueof the test signal within a valid sampling window is greater than the conformance limits of the $V_{OH\ (DC)}$ value specified in the JEDEC specification

Procedure:

1. Acquire and split read and write burst of the acquired signal.
2. Take the first valid READ burst found.
3. Find all valid positive pulses in the said burst. A valid positive pulse starts at V_{REF} crossing at valid rising edge and end at V_{REF} crossing at the following valid falling edge (See notes on "Threshold Settings" on page 69).
4. Zoom in on the first valid positive pulse and perform V_{TOP} measurement. Take the V_{TOP} measurement results as $V_{OH\ (DC)}$ value.
5. Continue the previous step with the rest of the valid positive pulses that were found in the burst.
6. Determine the worst result from the set of $V_{OH\ (DC)}$ measured.

Expected/Observable Results: The high level voltage value of the test signal shall be greater than or equal to the $V_{OH\ (DC)}$ value in the specification.

V_{OL} Test – AC Output Logic Low

V_{OL} Test can be divided into 2 sub tests: $V_{OL\ (AC)}$ test and $V_{OL\ (DC)}$.

$V_{OL\ (AC)}$ Test – AC Output Logic Low

Mode Supported: DDR4 , LPDDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signals (supported by Data Strobe Signals) OR
- Data Strobe Signals (supported by Data Signals)

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin is DQS or DQ depend on the PUT selected.

References:

Specifications document	Section#	Table#
DDR4 SDRAM Specification, JESD79-4, September 2012	8	Table 74
LPDDR4 SDRAM Specification, JESD209-4, August 2014	7.1.3.2	Table 69

Table 74 — Single-ended AC & DC output levels

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/3200	Units	NOTE
V_{OL}(AC)	AC output low measurement level (for output SR)	(0.7 - 0.15) x V_{DDQ}	V	1

Table 69 — Single-ended AC and DC Output Levels

Parameter	Symbol	Min	Max	Unit
Output high voltage	VOH	0.80 * V_{DD}Q	-	V
Output low voltage	VOL	-	0.20 * V_{DD}Q	V

Test Overview: The purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window is lower than the conformance lower limits of the $V_{OL\ (AC)}$ value specified in the JEDEC specification

Procedure:

1. Acquire and split read and write burst of the acquired signal.
2. Take the first valid READ burst found.
3. Find all valid negative pulses in the said burst. A valid negative pulse starts at V_{REF} crossing at valid falling edge and end at V_{REF} crossing at the following valid rising edge (See notes on "Threshold Settings" on page 69).

4 Zoom in on the first valid negative pulse and perform V_{BASE} measurement. Take the V_{BASE} measurement results as $V_{OL\ (AC)}$ value.

5 Continue the previous step with the rest of the valid negative pulses that were found in the burst.

6 Determine the worst result from the set of $V_{OL\ (AC)}$ measured.

Expected/Observable Results: The low level voltage value of the test signal shall be lower than or equal to the minimum $V_{OL\ (AC)}$ value.

$V_{OL\ (DC)}$ Test – DC Output Logic Low

Mode Supported: DDR4, LPDDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signals (supported by Data Strobe Signals) OR
- Data Strobe Signals (supported by Data Signals)

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin is DQS or DQ depend on the PUT selected.

References:

Specifications document	Section#	Table#
DDR4 SDRAM Specification, JESD79-4, September 2012	8	Table 74

Table 74 — Single-ended AC & DC output levels

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/3200	Units	NOTE
V_{OL}(DC)	DC output low measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V	

Test Overview: The purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window is lower than the conformance lower limits of the $V_{OL(DC)}$ value specified in the JEDEC specification

Procedure:

1 Acquire and split read and write burst of the acquired signal.

2 Take the first valid READ burst found.

3 Find all valid negative pulses in the said burst. A valid negative pulse starts at V_{REF} crossing at valid falling edge and end at V_{REF} crossing at the following valid rising edge (See notes on "Threshold Settings" on page 69).

4 Zoom in on the first valid negative pulse and perform V_{BASE} measurement. Take the V_{BASE} measurement results as $V_{OL\ (DC)}$ value.

5 Continue the previous step with the rest of the valid negative pulses that were found in the burst.

6 Determine the worst result from the set of $V_{OL\ (DC)}$ measured.

Expected/Observable Results: The low level voltage value of the test signal shall be lower than or equal to the minimum $V_{OL\ (DC)}$ value.

SRQseR – Output Signal Minimum Slew Rate (Rising)

Mode Supported: DDR4 , LPDDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signals (supported by Data Strobe Signals) OR
- Data Strobe Signals (supported by Data Signals)

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin is DQS or DQ depend on the PUT selected.

References:

Specifications document	Section#	Table#
DDR4 SDRAM Specification, JESD79-4, September 2012	8	Table 77
LPDDR4 SDRAM Specification, JESD209-4, August 2014	7.4	Table 74

Table 77 — Single-ended output slew rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-3200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	4	9	4	9	4	9	4	9	TBD	TBD	TBD	TBD	V/ns

Table 74 — Output Slew Rate (single-ended)

Parameter	Symbol	Value		Units
		Min[1]	Max[2]	
Single-ended Output Slew Rate (VOH = V_{DD}Q/3)	SRQse*	3.5	9	V/ns
Output slew-rate matching Ratio (Rise to Fall)	-	0.8	1.2	-
* SR = Slew Rate, Q = Query Output (like in DQ, which stands for Data-in, Query Output) se = Single-ended signals				

NOTE 1 Measured with output reference load.

NOTE 2 The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

NOTE 3 The output slew rate for falling and rising edges is defined and measured between VOL(AC)=0.2*VOH(DC) and VOH(AC)= 0.8*VOH(DC).

NOTE 4 Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

Test Overview: The purpose of this test is to verify that the rising slew rate value of the test signal is within the conformance limit of the SRQseR value specified in the JEDEC specification.

Procedure:

1. Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)
2. Take the first valid READ burst found.
3. Find all the valid rising edges in the said burst. A valid rising edge starts at $V_{OL\ (ac)}$ crossing and end at the following $V_{OH\ (ac)}$ crossing.
4. For all the valid rising edges, find the transition time, TR which is the time starts at $V_{OL\ (ac)}$ crossing and end at the following $V_{OH\ (ac)}$ crossing. Then calculate SRQseR = $[V_{OH\ (ac)} - V_{OL\ (ac)}]$ / TR.
5. Determine the worst result from the set of SRQseR measured.

Expected/Observable Results: The calculated Rising Slew/SRQseR value for the test signal shall be within the specification limit.

SRQseF – Output Signal Minimum Slew Rate (Falling)

Mode Supported: DDR4 , LPDDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signals (supported by Data Strobe Signals) OR
- Data Strobe Signals (supported by Data Signals) OR

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.

- Supporting Pin is DQS or DQ depend on the PUT selected.

References:

Specifications document	Section#	Table#
DDR4 SDRAM Specification, JESD79-4, September 2012	8	Table 77
LPDDR4 SDRAM Specification, JESD209-4, August 2014	7.4	Table 74

Table 77 — Single-ended output slew rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-3200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	4	9	4	9	4	9	4	9	TBD	TBD	TBD	TBD	V/ns

Table 74 — Output Slew Rate (single-ended)

Parameter	Symbol	Value		Units
		Min[1]	Max[2]	
Single-ended Output Slew Rate (VOH = $V_{DD}Q/3$)	SRQse*	3.5	9	V/ns
Output slew-rate matching Ratio (Rise to Fall)	-	0.8	1.2	-
* SR = Slew Rate, Q = Query Output (like in DQ, which stands for Data-in, Query Output) se = Single-ended signals				

NOTE 1 Measured with output reference load.

NOTE 2 The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

NOTE 3 The output slew rate for falling and rising edges is defined and measured between VOL(AC)=0.2*VOH(DC) and VOH(AC)= 0.8*VOH(DC).

NOTE 4 Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

Test Overview: The purpose of this test is to verify that the falling slew rate value of the test signal is within the conformance limit of the SRQseF value specified in the JEDEC specification.

Procedure:

1 Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)

2 Take the first valid READ burst found.

3 Find all the valid falling edges in the said burst. A valid falling edge starts at $V_{OH\ (ac)}$ crossing and end at the following $V_{OL\ (ac)}$ crossing.

4 For all the valid falling edges, find the transition time, TR which is the time starts at $V_{OH\ (ac)}$ crossing and end at the following $V_{OL\ (ac)}$ crossing. Then calculate SRQseF = $[V_{OH\ (ac)} - V_{OL\ (ac)}]$ / TR.

5 Determine the worst result from the set of SRQseF measured.

Expected/Observable Results: The calculated Falling Slew/SRQseF value for the test signal shall be within the specification limit.

AC Overshoot (amplitude, area)

Overshoot Test can be divided into 2 sub tests: Overshoot amplitude and Overshoot area.

Mode Supported: DDR4 , LPDDR4

Signal cycle of interest: READ or WRITE

Require Read/Write separation: No

Signal(s) of Interest:

- Data Signals OR
- Data Strobe Signals OR
- Address Signals OR
- Control Signals OR
- Data Mask Control Signals OR
- Clock Signals

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.

References:

Specifications document	Section#	Table#
DDR4 SDRAM Specification, JESD79-4, September 2012	7	Table 67, 68, and 69
LPDDR4 SDRAM Specification, JESD209-4, August 2014	7.1.4, 7.5	Table 70, Table 76

Table 67 — AC overshoot/undershoot specification for Address and Control pins

Parameter	Specification						Unit
	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-3200	
Maximum peak amplitude allowed for overshoot area	0.3	0.3	0.3	0.3	TBD	TBD	V
Maximum overshoot area above V_{DD}	0.25	0.25	0.25	TBD	TBD	TBD	V-ns

Table 69 — AC overshoot/undershoot specification for Data, Strobe and Mask

Parameter	Specification						Unit
	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-3200	
Maximum peak amplitude allowed for overshoot area	0.4	0.4	0.4	0.4	TBD	TBD	V
Maximum overshoot area above V_{DDQ}	0.2	0.2	0.2	0.2	TBD	TBD	V-ns

Table 68 — AC overshoot/undershoot specification for Clock

Parameter	Specification						Unit
	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-3200	
Maximum peak amplitude allowed for overshoot area	0.3	0.3	0.3	0.3	TBD	TBD	V
Maximum overshoot area above V_{DDQ}	0.10	0.10	0.10	TBD	TBD	TBD	V-ns

Table 70 — AC Overshoot/Undershoot Specification

Parameter	Specification
Maximum peak Amplitude allowed for overshoot area	0.35V
Maximum peak Amplitude allowed for undershoot area	0.35V
Maximum overshoot area above $V_{DD}/V_{DD}Q$	0.8V-ns
Maximum undershoot area below $V_{SS}/V_{SS}Q$	0.8V-ns

Table 76 — AC Overshoot/Undershoot Specification

Parameter		Data Rate				Units
		1600	1866	3200	4266	
Maximum peak amplitude allowed for overshoot area. (See Figure 102)	Max	0.3	0.3	0.3	TBD	V
Maximum peak amplitude allowed for undershoot area. (See Figure 102)	Max	0.3	0.3	0.3	TBD	V
Maximum area above V_{DD}. (See Figure 102)	Max	0.1	0.1	0.1	TBD	V-ns
Maximum area below V_{SS}. (See Figure 102)	Max	0.1	0.1	0.1	TBD	V-ns

NOTE 1 $V_{DD}2$ stands for V_{DD} for CA[5:0], CK_t, CK_c, CS_n, CKE and ODT. V_{DD} stands for $V_{DD}Q$ for DQ, DMI, DQS_t and DQS_c.

NOTE 2 VSS stands for VSS for CA[5:0], CK_t, CK_c, CS_n, CKE and ODT. V_{SS} stands for $V_{SS}Q$ for DQ, DMI, DQS_t and DQS_c.

NOTE 3 Maximum peak amplitude values are referenced from actual V_{DD} and V_{SS} values.

NOTE 4 Maximum area values are referenced from maximum operating V_{DD} and V_{SS} values.

Test Overview: The purpose of this test is to verify that the overshoot value of the test signal that found from all region of acquired waveform is lower than or equal to the conformance limit of the maximum peak amplitude allowed for overshoot as specified in the JEDEC specification.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude. The overshoot area should be lower than or equal to the conformance limit of the maximum overshoot area allowed as specified in the JEDEC specification.

Procedure:

1. Set the number of sampling points to 2M samples.
2. Sample/acquire signal data and then perform signal conditioning to maximize screen resolution (vertical scale adjustment).
3. Use T_{MAX}, V_{MAX} to get timestamp of maximum voltage on all region of acquired waveform.
4. Perform manual zoom waveform to maximum peak area
5. Find the edges before and after the Overshoot Point at the Supply Reference Level in order to calculate the maximum overshoot length duration. Table below shows the supply reference level for each pin group:

Pin	Supply Reference Level
DDR4 Address and Control pin.	VDD
DDR4 Data, Strobe and Mask pin.	VDDQ
DDR4 Clock	VDDQ
LPDDR4 XXXXXX	XXXXXX
LPDDR4 XXXXXX	XXXXXX

6. Calculate Overshoot Amplitude. Overshoot Amplitude = V_{MAX} - supply reference level (refer table above).
7. Calculate Overshoot area (V-ns)

   Area calculation is based on the area calculation of a triangle where the overshoot width is used as the triangle base and the overshoot amplitude is used as the triangle height.

   Area = 0.5 * base * height
8. Compare test result to the compliance test limit.

Expected/Observable Results:

- The measured maximum voltage value for the test signal shall be less than or equal to the maximum overshoot value.
- The calculated overshoot area value shall be less than or equal to the maximum overshoot area allowed.

AC Undershoot (amplitude, area)

Undershoot Test can be divided into 2 sub tests: Undershoot amplitude and Undershoot area

Mode Supported: DDR4 , LPDDR4

Signal cycle of interest: READ or WRITE

Require Read/Write separation: No

Signal(s) of Interest:

- Data Signals OR
- Data Strobe Signals OR
- Address Signals OR
- Control Signals OR
- Data Mask Control Signals OR
- Clock Signals

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.

References:

Specifications document	Section#	Table#
DDR4 SDRAM Specification, JESD79-4, September 2012	7	Table 67, 68, and 69

Table 67 — AC overshoot/undershoot specification for Address and Control pins

Parameter	Specification						Unit
	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-3200	
Maximum peak amplitude allowed for undershoot area	0.3	0.3	0.3	0.3	TBD	TBD	V
Maximum undershoot area below V_{SS}	0.25	0.25	0.25	TBD	TBD	TBD	V-ns

Table 69 — AC overshoot/undershoot specification for Data, Strobe and Mask

Parameter	Specification						Unit
	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-3200	
Maximum peak amplitude allowed for undershoot area	0.32	0.32	0.32	0.32	0	0	V
Maximum undershoot area below V_{SSQ}	0.1	0.1	0.1	0.1	0	0	V-ns

Table 68 — AC overshoot/undershoot specification for Clock

Parameter	Specification						Unit
	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-3200	
Maximum peak amplitude allowed for undershoot area	0.3	0.3	0.3	0.3	TBD	TBD	V
Maximum undershoot area below V_{SSQ}	0.10	0.10	0.10	TBD	TBD	TBD	V-ns

Test Overview: The purpose of this test is to verify that the undershoot value of the test signal that found from all region of acquired waveform is lower than or equal to the conformance limit of the maximum peak amplitude allowed for undershoot as specified in the JEDEC specification.

When there is undershoot, the undershoot area is calculated based on the undershoot width. The undershoot area should be lower than or equal to the conformance limit of the maximum undershoot area allowed as specified in the JEDEC specification.

Procedure:

1 Set the number of sampling points to 2M samples.
2 Sample/acquire signal data and then perform signal conditioning to maximize screen resolution (vertical scale adjustment).
3 Use T_{MIN}, V_{MIN} to get timestamp of minimum voltage on all region of acquired waveform.
4 Perform manual zoom waveform to minimum peak area
5 Find the edges before and after the Undershoot Point at the GND(~0V) level in order to calculate the maximum undershoot length duration.
6 Calculate Undershoot Amplitude. Undershoot Amplitude = 0 – V_{MIN}.
7 Calculate Undershoot area (V-ns)

   Area calculation is based on the area calculation of a triangle where the undershoot width is used as the triangle base and the undershoot amplitude is used as the triangle height.

   Area = 0.5 * base * height
8 Compare test result to the compliance test limit.

Expected/Observable Results:

- The measured minimum voltage value for the test signal shall be less than or equal to the maximum undershoot value.
- The calculated undershoot area value shall be less than or equal to the maximum undershoot area allowed.

V_{REF} Measurement

Mode Supported: DDR4

Signal cycle of interest: READ or WRITE

Require Read/Write separation: No

Signal(s) of Interest:

- V_{REF} Signal

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = V_{REF} Signal

References:

Specifications document	Section#
DDR4 SDRAM Specification, JESD79-4, September 2012	7

7.1 AC and DC Input Measurement Levels: V_{REF} Tolerances

The DC-tolerance limits and ac-noise limits for the reference voltages V_{REFCA} is illustrated in Figure 170. It shows a valid reference voltage $V_{REF}(t)$ as a function of time. (V_{REF} stands for V_{REFCA}).

$V_{REF}(DC)$ is the linear average of $V_{REF}(t)$ over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table X. Furthermore $V_{REF}(t)$ may temporarily deviate from $V_{REF}(DC)$ by no more than ± 1% V_{DD}.

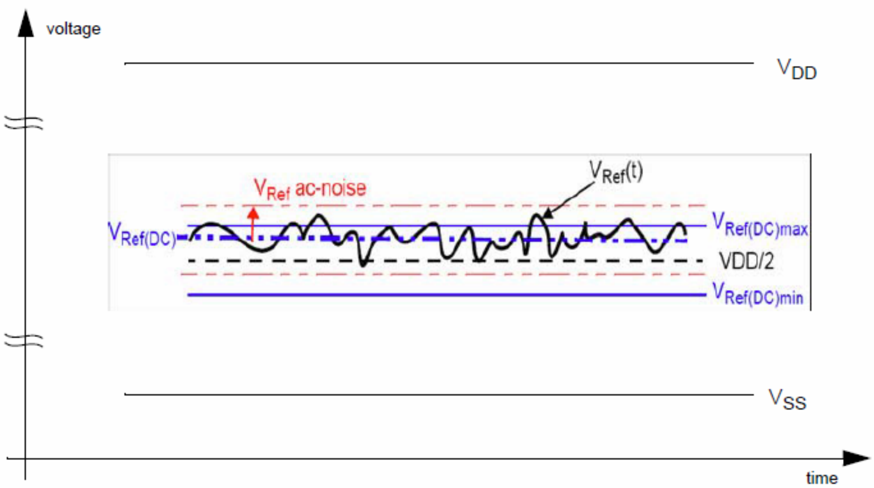


Figure 170 — Illustration of $V_{REF}(DC)$ tolerance and V_{REF} AC-noise limits

The voltage levels for setup and hold time measurements $V_{IH}(AC)$, $V_{IH}(DC)$, $V_{IL}(AC)$ and $V_{IL}(DC)$ are dependent on V_{REF}.

"V_{REF}" shall be understood as $V_{REF}(DC)$, as defined in Figure 170.

This clarifies, that DC-variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{REF}(DC)$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} AC-noise. Timing and voltage effects due to AC-noise on V_{REF} up to the specified limit (+/-1% of V_{DD}) are included in DRAM timings and their associated deratings.

Test Overview: The purpose of this test is to verify that the voltage level value of the V_{REF} signal is within the conformance limit of the V_{REF} value specified in the JEDEC specification.

Procedure:

1. Set the number of sampling points to 2M samples.
2. Sample/acquire signal data and then perform signal conditioning to maximize screen resolution (vertical scale adjustment).
3. Use T_{MAX}, V_{MAX} to get timestamp of maximum voltage on all region of acquired waveform.
4. Use T_{MIN}, V_{MIN} to get timestamp of minimum voltage on all region of acquired waveform.
5. Take V_{MIN} or V_{MAX} for the worst test result.

6 Compare test result to the compliance test limit.

Expected/Observable Results: The worst voltage level of the V_{REF} signal shall be within the specification limit.

Differential Signals Tests

Differential AC and DC Input Levels for Clock

Differential AC Input Levels for Clock can be divided into these sub tests: $V_{IHdiff.CK\ (AC)}$ test, $V_{ILdiff.CK\ (AC)}$ test, $V_{IHdiff.CK\ (DC)}$ test, and $V_{ILdiff.CK\ (DC)}$ test.

$V_{IHdiff.CK\ (AC)}$ – Differential Input High AC for Clock

Mode Supported: DDR4, LPDDR4

Signal cycle of interest: READ or WRITE

Require Read/Write separation: No

Signal(s) of Interest:

- Clock Signals

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.

References:

Specifications document	Section#	Table#
DDR4 SDRAM Specification, JESD79-4, September 2012	7	Table 64
LPDDR4 SDRAM Specification, JESD209-4, August 2014	-	-

Table 64 — Differential AC and DC Input Levels

Symbol	Parameter	DDR4 -1600,1866,2133		DDR4 -2400,2666 & 3200		unit	NOTE
		min	max	min	max		
V_{IHdiff}(AC)	differential input high ac	2 x (V_{IH}(AC) - V_{REF})	NOTE 3	2 x (V_{IH}(AC) - V_{REF})	NOTE 3	V	2

Test Overview: The purpose of this test is to verify that the high level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{IHdiff\ (AC)}$ value as specified in the JEDEC specification.

Procedure:

1. Pre-condition the oscilloscope.
2. Trigger on the rising edge of the clock signal under test.
3. Find all valid Clock positive pulse in the triggered waveform. A valid Clock positive pulse starts at 0 Volt crossing at valid Clock rising edge and end at 0

Volt crossing at following valid Clock falling edge (See notes on "Threshold Settings" on page 69).

4 Zoom into the first pulse and perform V_{TOP}. Take the V_{TOP} measurement as $V_{IHdiff\ (AC)}$ value.

5 Continue the previous step with another 9 valid positive pulses found in the said waveform.

6 Determine the worst result from the set of $V_{IHdiff\ (AC)}$ measured.

Expected/Observable Results: The worst measured $V_{IHdiff\ (AC)}$ shall be within the specification limit.

$V_{ILdiff.CK\ (AC)}$ – Differential Input Low AC for Clock

Mode Supported: DDR4, LPDDR4

Signal cycle of interest: READ or WRITE

Require Read/Write separation: No

Signal(s) of Interest:

- Clock Signals

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.

References:

Specifications document	Section#	Table#
DDR4 SDRAM Specification, JESD79-4, September 2012	7	Table 64
LPDDR4 SDRAM Specification, JESD209-4, August 2014	-	-

Table 64 — Differential AC and DC Input Levels

Symbol	Parameter	DDR4 -1600,1866,2133		DDR4 -2400,2666 & 3200		unit	NOTE
		min	max	min	max		
V_{ILdiff}(AC)	differential input low ac	NOTE 3	2 x (V_{IL}(AC) - V_{REF})	NOTE 3	2 x (V_{IL}(AC) - V_{REF})	V	2

Test Overview: The purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{ILdiff\ (AC)}$ value as specified in the JEDEC specification.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the clock signal under test.

3 Find all valid Clock negative pulse in the triggered waveform. A valid Clock negative pulse starts at 0 Volt crossing at valid Clock falling edge and end at 0 Volt crossing at following valid Clock rising edge (See notes on "Threshold Settings" on page 69).

4 Zoom into the first pulse and perform V_{BASE}. Take the V_{BASE} measurement as $V_{ILdiff\ (AC)}$ value.

5 Continue the previous step with another 9 valid positive pulses found in the said waveform.

6 Determine the worst result from the set of $V_{ILdiff\ (AC)}$ measured.

Expected/Observable Results: The worst measured $V_{ILdiff\ (AC)}$ shall be within the specification limit.

$V_{IHdiff.CK\ (DC)}$ – Differential Input High DC for Clock

Mode Supported: DDR4, LPDDR4

Signal cycle of interest: READ or WRITE

Require Read/Write separation: No

Signal(s) of Interest:

- Clock Signals

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the high level voltage value of the test signal within a valid sampling window. The limit is definable by the customers for their evaluation tests usage.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the clock signal under test.

3 Find all valid Clock positive pulse in the triggered waveform. A valid Clock positive pulse starts at 0 Volt crossing at valid Clock rising edge and end at 0 Volt crossing at following valid Clock falling edge (See notes on "Threshold Settings" on page 69).

4 Zoom into the first pulse and perform V_{TOP}. Take the V_{TOP} measurement as $V_{IHdiff\ (DC)}$ value.

5 Continue the previous step with another 9 valid positive pulses found in the said waveform.

6 Determine the worst result from the set of $V_{IHdiff\ (DC)}$ measured.

Expected/Observable Results: The worst measured $V_{IHdiff (DC)}$ shall meet the user defined limit.

$V_{ILdiff.CK (DC)}$ – Differential Input Low DC for Clock

Mode Supported: DDR4, LPDDR4

Signal cycle of interest: READ or WRITE

Require Read/Write separation: No

Signal(s) of Interest:

- Clock Signals

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the low level voltage value of the test signal within a valid sampling window. The limit is definable by the customers for their evaluation tests usage.

Procedure:

1 Pre-condition the oscilloscope.
2 Trigger on the rising edge of the clock signal under test.
3 Find all valid Clock negative pulse in the triggered waveform. A valid Clock negative pulse starts at 0 Volt crossing at valid Clock falling edge and end at 0 Volt crossing at following valid Clock rising edge (See notes on "Threshold Settings" on page 69).
4 Zoom into the first pulse and perform V_{BASE}. Take the V_{BASE} measurement as $V_{ILdiff (DC)}$ value.
5 Continue the previous step with another 9 valid positive pulses found in the said waveform.
6 Determine the worst result from the set of $V_{ILdiff (DC)}$ measured.

Expected/Observable Results: The worst measured $V_{ILdiff (DC)}$ shall meet the user defined limit.

Differential AC Input Levels for Strobe

Differential AC Input Levels for Strobe can be divided into these sub tests: $V_{IHdiff.DQS (AC)}$ test, $V_{ILdiff.DQS (AC)}$ test, $V_{IHdiff.DQS (DC)}$ test, and $V_{ILdiff.DQS (DC)}$ test

$V_{IHdiff.DQS (AC)}$ – Differential Input High AC for Strobe

Mode Supported: DDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signals (supported by Data Signals)

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin = DQ

References:

Specifications document	Section#	Table#
DDR4 SDRAM Specification, JESD79-4, September 2012	7	Table 64

Table 64 — Differential AC and DC Input Levels

Symbol	Parameter	DDR4 -1600,1866,2133		DDR4 -2400,2666 & 3200		unit	NOTE
		min	max	min	max		
$V_{IHdiff}(AC)$	differential input high ac	2 x (V_{IH}(AC) - V_{REF})	NOTE 3	2 x (V_{IH}(AC) - V_{REF})	NOTE 3	V	2

Test Overview: The purpose of this test is to verify that the high level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{IHdiff\ (AC)}$ value as specified in the JEDEC specification.

Procedure:

1. Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)
2. Take the first valid WRITE burst found.
3. Find all valid Strobe positive pulse in the said burst. A valid Strobe positive pulse starts at 0 Volt crossing at valid Strobe rising edge and end at 0 Volt crossing at following valid Strobe falling edge (See notes on "Threshold Settings" on page 69).
4. Zoom into the first pulse and perform V_{TOP}. Take the V_{TOP} measurement as $V_{IHdiff\ (AC)}$ value.
5. Continue previous step with the rest of the positive pulses in the said burst.
6. Determine the worst result from the set of $V_{IHdiff\ (AC)}$ measured.

Expected/Observable Results: The worst measured $V_{IHdiff\ (AC)}$ shall be within the specification limit.

$V_{ILdiff.DQS\ (AC)}$ – Differential Input Low AC for Strobe

Mode Supported: DDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signals (supported by Data Signals)

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin = DQ

References:

Specifications document	Section#	Table#
DDR4 SDRAM Specification, JESD79-4, September 2012	7	Table 64

Table 64 — Differential AC and DC Input Levels

Symbol	Parameter	DDR4 -1600,1866,2133		DDR4 -2400,2666 & 3200		unit	NOTE
		min	max	min	max		
V_{ILdiff}(AC)	differential input low ac	NOTE 3	2 x (V_{IL}(AC) - V_{REF})	NOTE 3	2 x (V_{IL}(AC) - V_{REF})	V	2

Test Overview: The purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{ILdiff\ (AC)}$ value as specified in the JEDEC specification.

Procedure:

1. Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)
2. Take the first valid WRITE burst found.
3. Find all valid Strobe negative pulse in the said burst. A valid Strobe negative pulse starts at 0 Volt crossing at valid Strobe falling edge and end at 0 Volt crossing at following valid Strobe rising edge (See notes on "Threshold Settings" on page 69).
4. Zoom into the first pulse and perform V_{BASE}. Take the V_{BASE} measurement as $V_{ILdiff\ (AC)}$ value.
5. Continue previous step with the rest of the negative pulses in the said burst.
6. Determine the worst result from the set of $V_{ILdiff\ (AC)}$ measured.

Expected/Observable Results: The worst measured $V_{ILdiff\,(AC)}$ shall be within the specification limit.

$V_{IHdiff.DQS\,(DC)}$ – Differential Input High DC for Strobe

Mode Supported: DDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signals (supported by Data Signals)

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin = DQ

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the high level voltage value of the test signal within a valid sampling window. The limit is definable by the customers for their evaluation tests usage.

Procedure:

1 Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)

2 Take the first valid WRITE burst found.

3 Find all valid Strobe positive pulse in the said burst. A valid Strobe positive pulse starts at 0 Volt crossing at valid Strobe rising edge and end at 0 Volt crossing at following valid Strobe falling edge (See notes on "Threshold Settings" on page 69).

4 Zoom into the first pulse and perform V_{TOP}. Take the V_{TOP} measurement as $V_{IHdiff\,(DC)}$ value.

5 Continue previous step with the rest of the positive pulses in the said burst.

6 Determine the worst result from the set of $V_{IHdiff\,(DC)}$ measured.

Expected/Observable Results: The worst measured $V_{IHdiff\,(DC)}$ shall meet the user defined limit.

$V_{ILdiff.DQS\,(DC)}$ – Differential Input Low DC for Strobe

Mode Supported: DDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:
- Data Strobe Signals (supported by Data Signals)

Required Signals: Needed to perform this test on oscilloscope:
- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin = DQ

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the low level voltage value of the test signal within a valid sampling window. The limit is definable by the customers for their evaluation tests usage.

Procedure:
1. Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)
2. Take the first valid WRITE burst found.
3. Find all valid Strobe negative pulse in the said burst. A valid Strobe negative pulse starts at 0 Volt crossing at valid Strobe falling edge and end at 0 Volt crossing at following valid Strobe rising edge (See notes on "Threshold Settings" on page 69).
4. Zoom into the first pulse and perform V_{BASE}. Take the V_{BASE} measurement as $V_{ILdiff\ (DC)}$ value.
5. Continue previous step with the rest of the negative pulses in the said burst.
6. Determine the worst result from the set of $V_{ILdiff\ (DC)}$ measured.

Expected/Observable Results: The worst measured $V_{ILdiff\ (DC)}$ shall meet the user defined limit.

Vix – AC Differential Cross Point Voltage for Clock

Mode Supported: DDR4

Signal cycle of interest: WRITE

Require Read/Write separation: No

Signal(s) of Interest:
- Clock Signals

Required Signals: Needed to perform this test on oscilloscope:
- Pin Under Test, PUT = Clock Signals.

References:

Specifications document	Section#	Table#
DDR4 SDRAM Specification, JESD79-4, September 2012	7	Table 71

Table 71 — Cross point voltage for differential input signals (CK)

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/3200		Unit	Note
		min	max		
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c	-120	-120	mV	2
		-TBD	-TBD	mV	1

Test Overview: The purpose of this test is to verify crossing point voltage value of the input differential pair test signals is within the conformance limits of the $V_{IX\ (CK)}$ as specified in the JEDEC specification.

Procedure:

1. Sample/Acquire data waveforms.
2. Use Subtract FUNC to generate the differential waveform from the 2 source input
3. Find all differential CLK crossing that cross 0V.
4. Use VTime to get the actual crossing point voltage value using the timestamp obtained
5. For each cross point voltage, calculate the final result. $V_{IX\ (ac)}$ = cross point voltage - VDD/2.
6. Determine the worst result from the set of $V_{IX\ (ac)}$ measured.

Expected/Observable Results: The measured crossing point value for the differential test signals pair shall be within the conformance limit of the VIX(CK) value.

Differential AC Output Levels

Differential AC Output Levels can be divided into 2 sub tests: $V_{OHdiff\ (AC)}$ test and $V_{OLdiff\ (AC)}$ test

$V_{OHdiff\ (AC)}$ – AC Differential Output High Measurement Level

Mode Supported: DDR4, LPDDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:
- Data Strobe Signals (supported by Data Signals)

Required Signals: Needed to perform this test on oscilloscope:
- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin = DQ

References:

Specifications document	Section#	Table#
DDR4 SDRAM Specification, JESD79-4, September 2012	8	Table 75

Table 75 — Differential AC & DC output levels

Symbol	Parameter	DDR4-1600/1866/2133/2400/ 2666/3200	Units	NOTE
V_{OHdiff}(AC)	AC differential output high measurement level (for output SR)	+0.3 x V_{DDQ}	V	1

Test Overview: The purpose of this test is to verify that the high level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{OHdiff\ (AC)}$ value as specified in the JEDEC specification.

Procedure:
1. Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)
2. Take the first valid READ burst found.
3. Find all valid Strobe positive pulse in the said burst. A valid Strobe positive pulse starts at 0 Volt crossing at valid Strobe rising edge and end at 0 Volt crossing at following valid Strobe falling edge (See notes on "Threshold Settings" on page 69).
4. Zoom into the first pulse and perform V_{TOP}. Take the V_{TOP} measurement as $V_{OHdiff\ (AC)}$ value.
5. Continue previous step with the rest of the positive pulses in the said burst.
6. Determine the worst result from the set of $V_{OHdiff\ (AC)}$ measured.

Expected/Observable Results: The worst measured $V_{OHdiff\ (AC)}$ shall be within the specification limit.

$V_{OLdiff\ (AC)}$ – AC Differential Output Low Measurement Level

Mode Supported: DDR4, LPDDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signals (supported by Data Signals)

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin = DQ

References:

Specifications document	Section#	Table#
DDR4 SDRAM Specification, JESD79-4, September 2012	8	Table 75

Table 75 — Differential AC & DC output levels

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/3200	Units	NOTE
$V_{OLdiff}(AC)$	AC differential output low measurement level (for output SR)	-0.3 x V_{DDQ}	V	1

Test Overview: The purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{OLdiff\ (AC)}$ value as specified in the JEDEC specification.

Procedure:

1. Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)
2. Take the first valid READ burst found.
3. Find all valid Strobe negative pulse in the said burst. A valid Strobe negative pulse starts at 0 Volt crossing at valid Strobe falling edge and end at 0 Volt crossing at following valid Strobe rising edge (See notes on "Threshold Settings" on page 69).
4. Zoom into the first pulse and perform V_{BASE}. Take the V_{BASE} measurement as $V_{OLdiff\ (AC)}$ value.
5. Continue previous step with the rest of the negative pulses in the said burst.
6. Determine the worst result from the set of $V_{OLdiff\ (AC)}$ measured.

Expected/Observable Results: The worst measured $V_{OLdiff\ (AC)}$ shall be within the specification limit.

Differential Output Slew Rate

Differential Output Slew Rate can be divided into 2 sub tests: SRQdiffR test and SRQdiffF test

SRQdiffR – Differential Output Slew Rate for Rising Edge

Mode Supported: DDR4 , LPDDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:
- Data Strobe Signals (supported by Data Signals)

Required Signals: Needed to perform this test on oscilloscope:
- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin = DQ

References:

Specifications document	Section#	Table#	Figure#
DDR4 SDRAM Specification, JESD79-4, September 2012	8	Table 79	
LPDDR4 SDRAM Specification, JESD209-4, August 2014	7.4	Table 75	Figure 101

Table 79 — Differential output slew rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-3200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Differential output slew rate	SRQdiff	8	18	8	18	8	18	8	18	TBD	TBD	TBD	TBD	V/ns

Table 75 — Differential Output Slew Rate

Parameter	Symbol	Value		Units
		Min	Max	
Differential Output Slew Rate (VOH=V_{DD}Q/3)	SRQdiff*	7	18	V/ns
* SR = Slew Rate, Q = Query Output (like in DQ, which stands for Data-in, Query Output) diff = Differential signals				

NOTE 1 Measured with output reference load.

NOTE 2 The output slew rate for falling and rising edges is defined and measured between VOL(AC)=0.2*VOH(DC) and VOH(AC)= 0.8*VOH(DC).

NOTE 3 Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

Test Overview: The purpose of this test is to verify that the differential output slew rate for rising edge of the test signal must be within the conformance limit of the SRQdiff value as specified in the JEDEC specification.

Procedure:

1 Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)

2 Take the first valid READ burst found.

3 Find all valid Strobe rising edge in the said burst. A valid Strobe rising edge starts at $V_{OLdiff\ (AC)}$ crossing and end at following $V_{OHdiff\ (AC)}$ crossing.

4 For all Strobe valid rising edge, find the transition time, TR which is time starts at $V_{OLdiff\ (AC)}$ crossing and end at following $V_{OHdiff\ (AC)}$ crossing. Then calculate SRQdiffR = [$V_{OHdiff\ (AC)}$ - $V_{OLdiff\ (AC)}$] / TR.

5 Determine the worst result from the set of SRQdiffR measured.

Expected/Observable Results: The worst measured SRQdiffR shall be within the specification limit.

SRQdiffF – Differential Output Slew Rate for Falling Edge

Mode Supported: DDR4 , LPDDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signals (supported by Data Signals)

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin = DQ

References:

Specifications document	Section#	Table#	Figure#
DDR4 SDRAM Specification, JESD79-4, September 2012	8	Table 79	
LPDDR4 SDRAM Specification, JESD209-4, August 2014	7.4	Table 75	Figure 101

Table 79 — Differential output slew rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-3200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Differential output slew rate	SRQdiff	8	18	8	18	8	18	8	18	TBD	TBD	TBD	TBD	V/ns

Table 75 — Differential Output Slew Rate

Parameter	Symbol	Value		Units
		Min	Max	
Differential Output Slew Rate (VOH=V_{DD}Q/3)	SRQdiff*	7	18	V/ns
* SR = Slew Rate, Q = Query Output (like in DQ, which stands for Data-in, Query Output) diff = Differential signals				

NOTE 1 Measured with output reference load.

NOTE 2 The output slew rate for falling and rising edges is defined and measured between VOL(AC)=0.2*VOH(DC) and VOH(AC)= 0.8*VOH(DC).

NOTE 3 Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

Test Overview: The purpose of this test is to verify that the differential output slew rate for falling edge of the test signal must be within the conformance limit of the SRQdiff value as specified in the JEDEC specification.

Procedure:

1. Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)
2. Take the first valid READ burst found.
3. Find all valid Strobe falling edge in the said burst. A valid Strobe falling edge starts at $V_{OHdiff\ (AC)}$ crossing and end at following $V_{OLdiff\ (AC)}$ crossing.
4. For all Strobe valid falling edge, find the transition time, TR which is time starts at $V_{OHdiff\ (AC)}$ crossing and end at following $V_{OLdiff\ (AC)}$ crossing. Then calculate SRQdiffF = [$V_{OHdiff\ (AC)}$ - $V_{OLdiff\ (AC)}$] / TR.
5. Determine the worst result from the set of SRQdiffF measured.

Expected/Observable Results: The worst measured SRQdiffF shall be within the specification limit.

5 Timing Tests Group

KEYSIGHT TECHNOLOGIES

Overview

The following groups of tests pertain to the timing operating conditions of a DDR4 DRAM as defined in JEDEC specification. The tests consist of simple triggering test which further divided into Clock Timing Tests, Data Strobe Timing Tests, Data Mask Timing Tests, and Command & Address Timing Test.

DDR Read/Write Separation

It is essential to separate read and write bursts for most of the timing parameters to be measured in the appropriate read or write cycle. Two signals are needed, DQS and DQ. The following flow chart shows the process of splitting read and write.

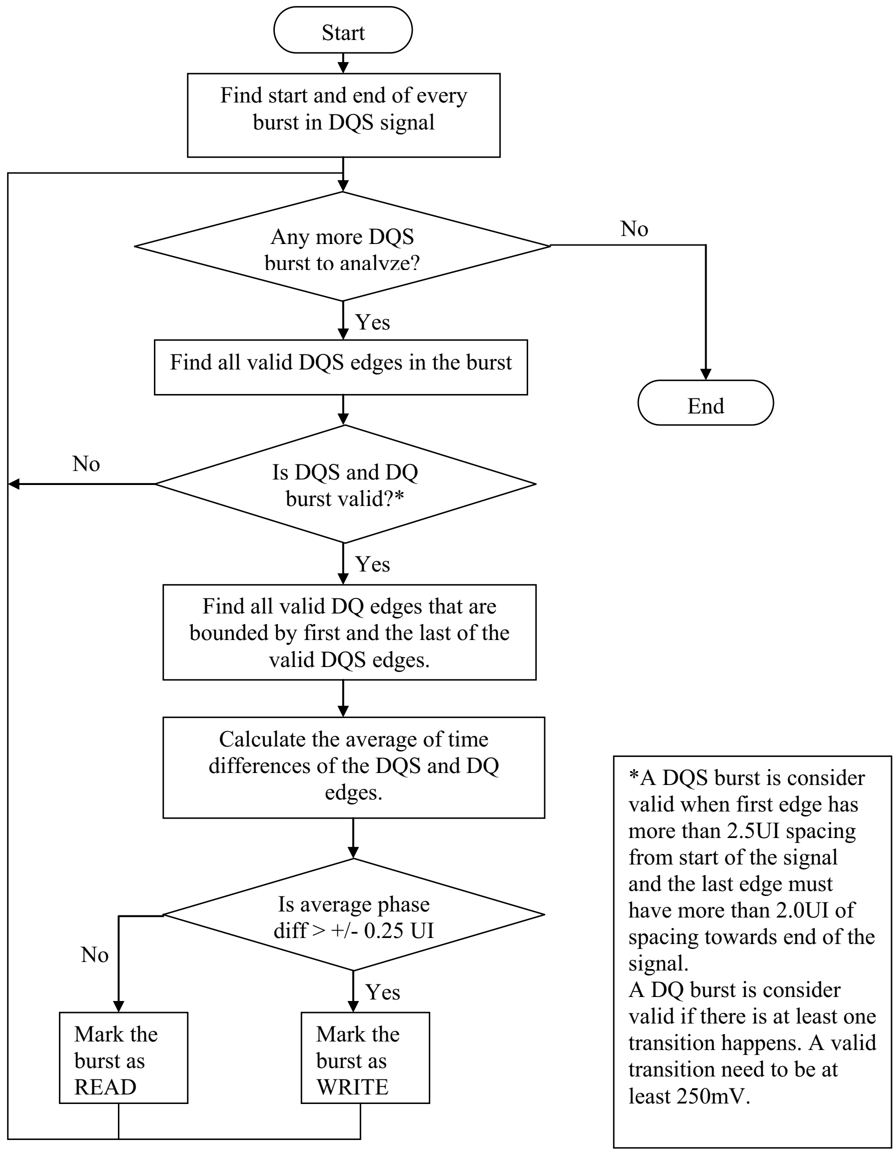
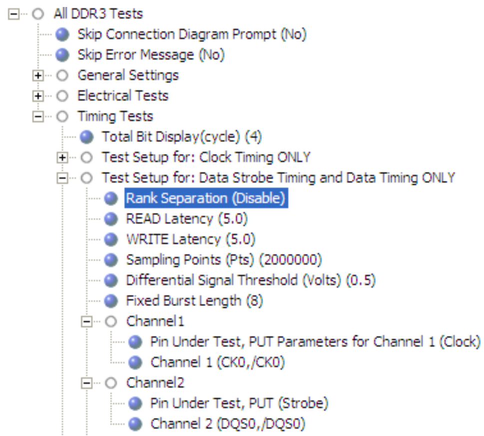
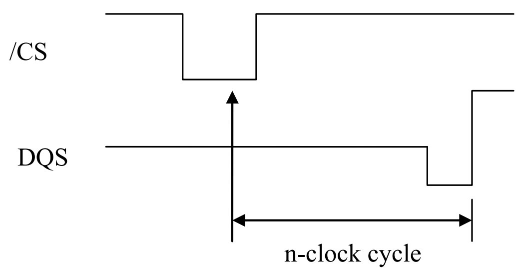


Figure 4 Flowchart for the Read/Write separation process

Filtering by specifying Latency Value



Read and write burst can be further filtered by specifying the latency value. If "Rank Separation" option is enabled, "READ Latency" and "WRITE Latency" values will be used to determine if a READ burst or WRITE burst will be used in further measurement. The following diagram shows how Latency is measured.

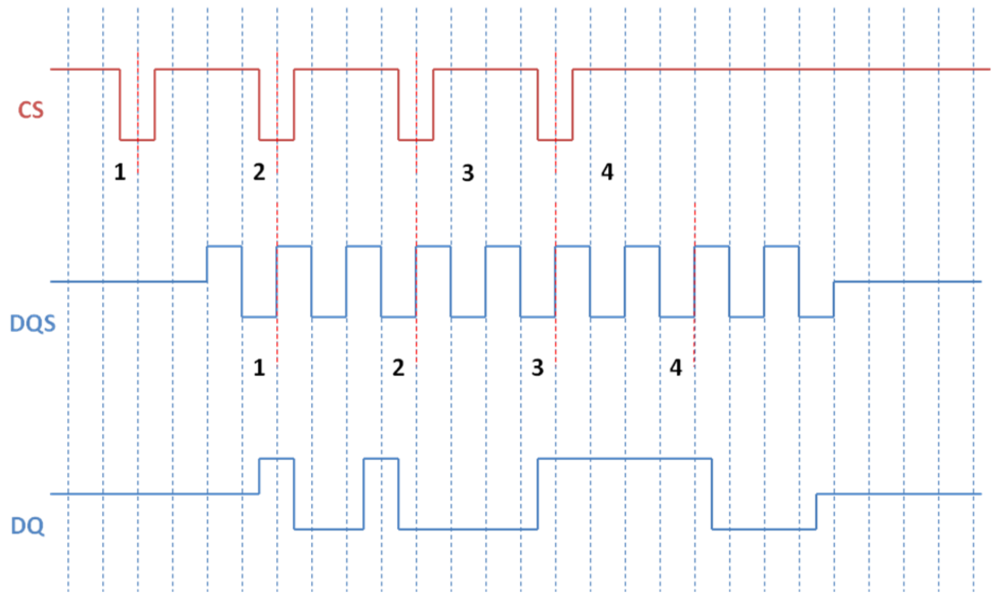


/CS will be sampled at n-clock cycle from first edge of DQS. n refers to the READ or WRITE latency set depends on the burst. /CS must be low to fulfill the filter criteria. /CS high at sample time will be rejected.

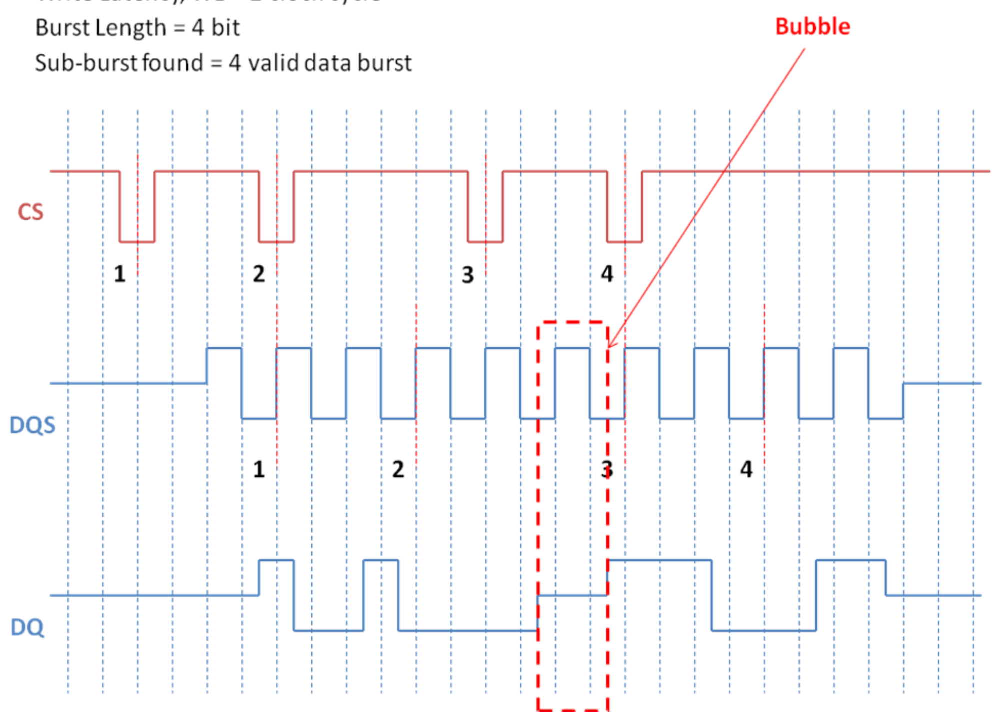
Handling DDR4 back-to-back WRITE burst data

One of the challenges in handling the WRITE data burst of a DDR4 signal is to be able to correctly identify the start bit and end bit position of the data burst. This task is particularly difficult to perform during a back-to-back WRITE data burst due to the WRITE preamble pattern (as defined in the JEDEC specs). The WRITE preamble pattern will cause multiple back-to-back bursts seem like one continuous long burst with/without bubble states (the preamble region). Examples of the back-to-back WRITE data burst are shown in the following figures.

Write Latency, WL = 2 clock cycle
Burst Length = 4 bit
Sub-burst found = 4 valid data burst



Write Latency, WL = 2 clock cycle
Burst Length = 4 bit
Sub-burst found = 4 valid data burst



In order to eliminate the bubble states (if any) during a back-to-back WRITE data burst, the Chip Select signal is required to identify the valid start bit of every data burst(or called sub-burst) within a continuous back-to-back WRITE data burst. A few assumptions are used in this approach as follow.

1. CS will be low during chained bursts to indicate a read or write command.
2. All burst are the same length, that is, in a captured waveform, only one burst length is used for all single burst data or multiple back-to-back burst data.
3. Back-to-back burst data are applicable for only one rank at a time, that is, all the multiple burst data in a back-to-back burst are only meant for one single rank/DIMM at a time.
4. In a back-to-back burst data, there will be only ONE bubble bit (if any) between any 2 consecutive burst data. For example (fix burst length=8 bit data), at the end of a the first burst data (within a long back-to-back burst),i.e the 8th bit data, a bubble state(if any) can be verified by checking the 9th bit data against the CS signal. If a bubble state exists, then the 9th and 10th bit of the DQS will be ignored and the 11th bit data will mark the beginning of a new burst data. The 11th bit data should have a corresponding CS low to indicate it is a valid consecutive burst data. The process will repeat for all the multiple bursts within the back-to-back burst data.

Assumption #1 indicate a limitation on this approach to handle the back-to-back burst because a logic low on the CS signal does not necessary means that it is a WRITE/READ command being issued. A logic low state on the CS signal can be due to other commands (such as PRECHARGE, REFRESH, etc) being issued. Therefore when there are 2 consecutive low states on the CS signal during a back-to-back burst transition, all the data bits of the burst data from that point onwards will be ignored.

Assumption #2 also indicate a limitation on this approach to handle the back-to-back burst because it cannot support any variable burst length waveform data as allowed in DDR4. DDR4 users that change the burst length on the fly (4-bit data to 8-bit data or vice-versa using A12) will not be supported even though it is a valid feature as specified in the JEDEC specs.

A general description on the actual algorithm to handle the DDR4 back-to-back WRITE data burst is explained as follow (fixed burst length = 8 bit).

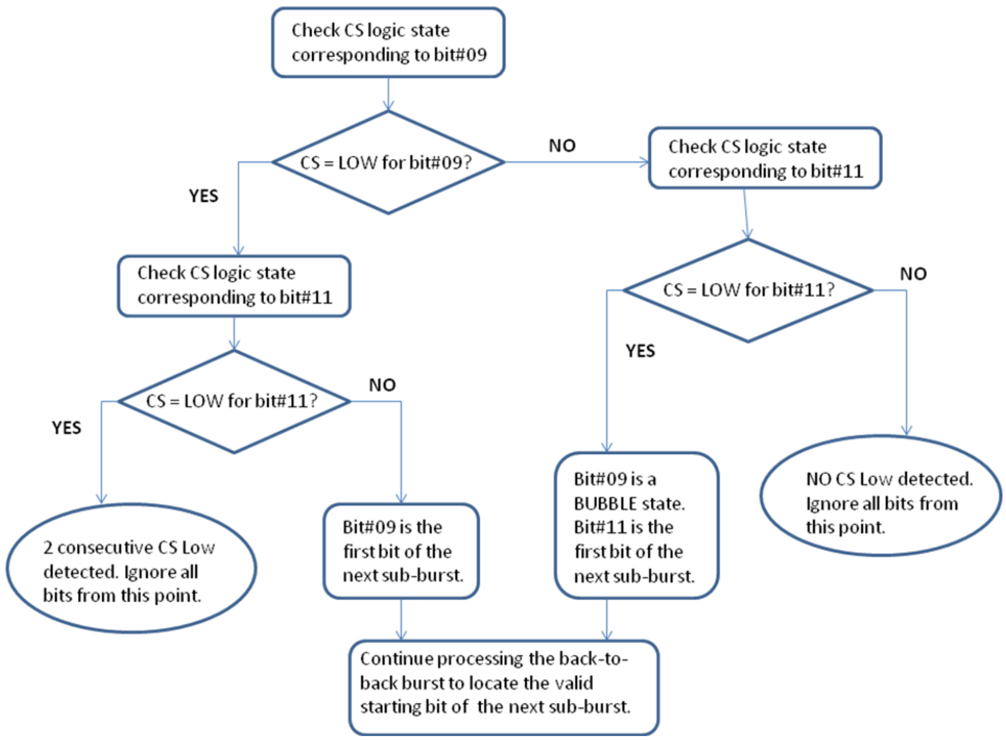
1. Starting from bit#1(of the long burst data), the expected starting bit of the next burst will be bit#9(Bit#1 + 8 Bit length).
2. Bit#9 will be check against the CS signal to see if there is a CS low assertion at the latency delay interval.
3. If there are no valid CS low assertion found, then bit#9 is a bubble state and the starting bit of the next burst will be bit#11(rising edge).

   If there is a valid CS low assertion found, then the next rising edge DQS (bit#11) will be check against the CS signal to see if there is a CS low assertion.

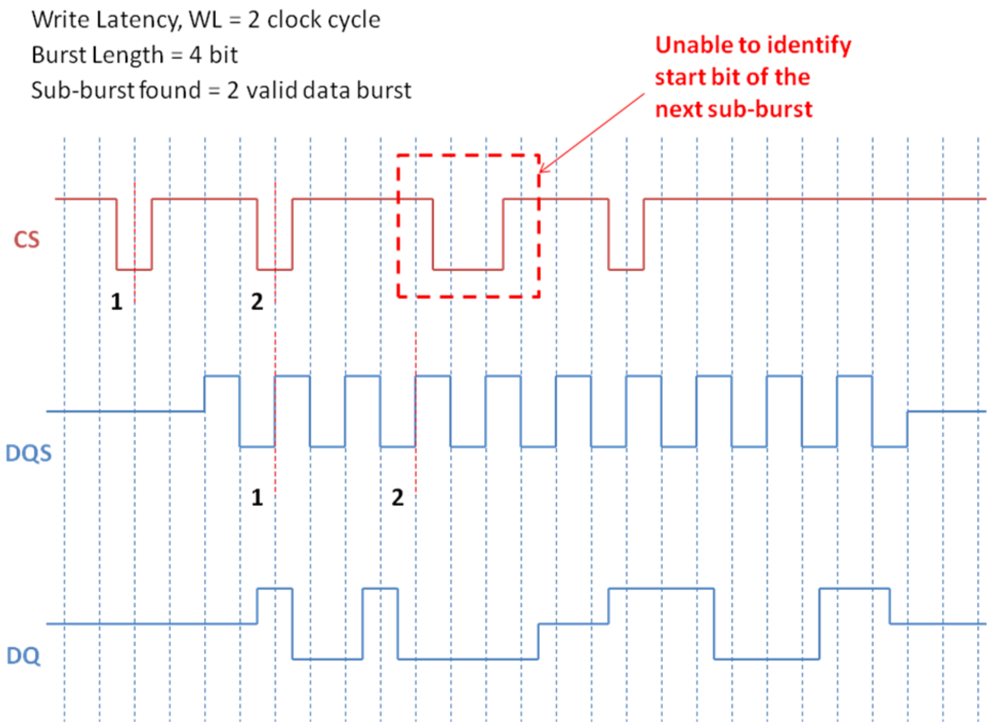
4 If there is a valid CS low assertion found (correspond to Bit#11), then due to the 2 consecutive CS low detected (for Bit#9 and Bit#11), all data bits from this point will be ignored.

   But if there are no CS low assertion found (correspond to Bit#11), then bit#9 is a valid starting bit of a burst.

5 The new expected starting bit for a burst will be checked by repeating procedure 'a'(if the current starting bit is Bit#9, then the next expected burst will be Bit#17).



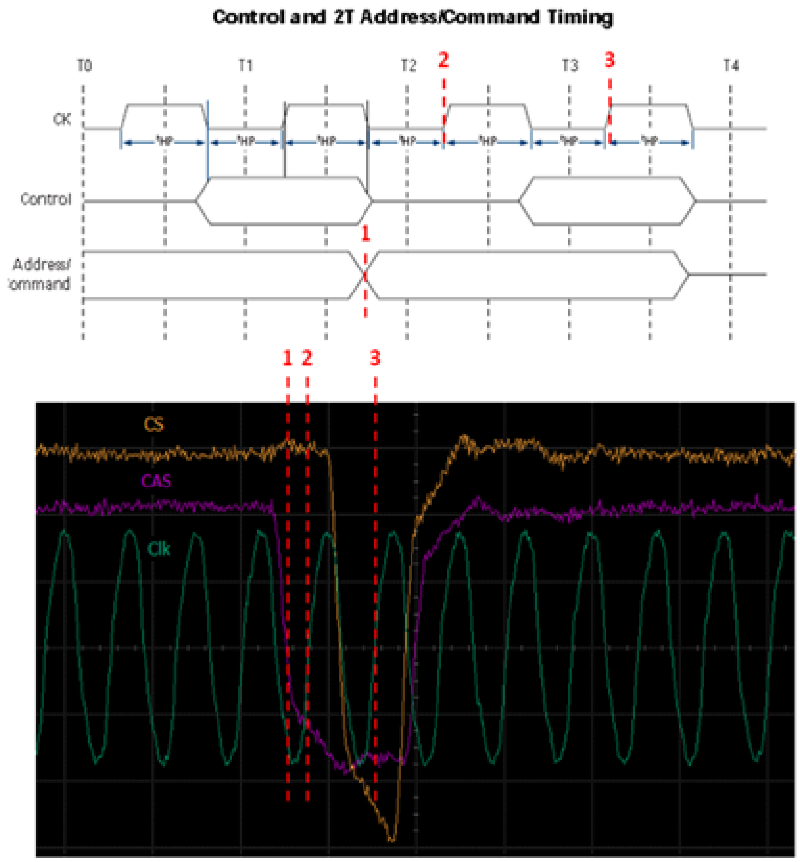
This approach includes every possible bit for a DDR4 back-to-back WRITE burst, EXCEPT the conditions when another command (for example, "PRECHARGE" or "REFRESH" command) happens in the midst of back-to-back bursts. When that happens, the chip select signal is asserted for two clock cycles and therefore we cannot identify which of the two marks the WRITE command. Due to that characteristic, we will not be able to correctly identify which state is the "bubble state". All the data bits from that point onwards will be ignored for the processed data burst. An example of this scenario is shown in the figure below where only two sub-bursts are able to be identified from the back-to-back WRITE data burst.



Handling DDR4 "2T timing" for tIS/tIS(derate) test

A config option to enable/disable the "2T timing" mode is available under the config tab (Timing Tests >Test Setup for: Command and Address Timing ONLY), namely "Clocking Method".

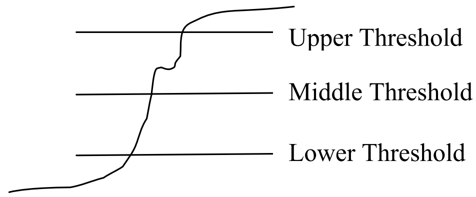
For this "2T timing" support feature approach, the main idea is to have the app to use the second closest rising clock edge(instead of the closest rising edge in the typical "1T timing") with reference to the CA (Command/Address) edge when processing the tIS/tIS(derate) test. For example illustration purposes, the screenshot of a sample waveforms from AMD below shows the impact of enabling the "2T timing" feature.



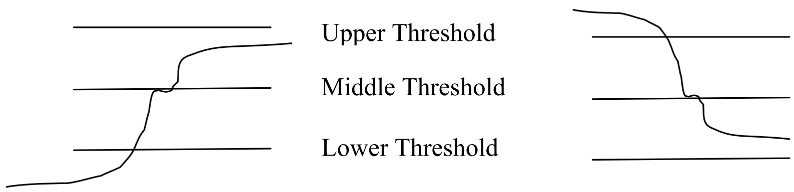
Based on the attached figure, the tIS/tIS(derate) test will measure the time difference between line position #1 and #2 under normal "1T timing" operation mode. For "2T timing" operation mode, the app will measure the time difference between line position #1 and #3 instead. One main assumption in this approach is that the transition edge of the CA PUT will occur before line position #2 (as it should). If the CA transition edge is to occur after line position #2 for any reason (very bad slew or signal integrity issue), then this approach will not work. So far (as at 15/Dec/2010), we haven't seen any of those cases yet (or know whether those scenario exist at all), but this is a limitation of this implementation approach. The approach here should work well with the current AMD signals (based on the given waveform files) and also any typical DDR DUT system working under the "2T timing" operation mode.

Threshold Settings

Most of the timing tests are utilizing the threshold settings for determines if an edge is indeed a valid edge. In general, an edge must past 3 levels of threshold to qualify as an edge as shown.



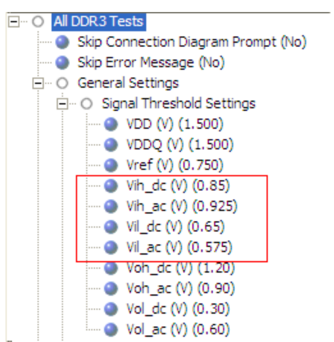
Valid edge



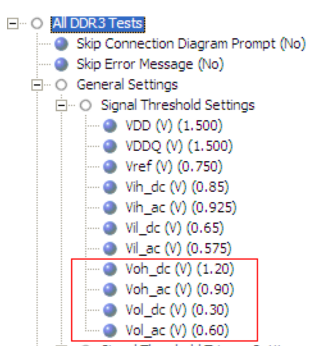
Invalid edges

The application provides 2 methods for setting the threshold levels.

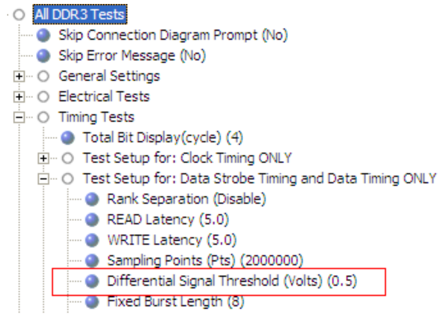
Method 1 This section will set the threshold settings for all single-ended signals except for Data signal of READ burst and single-ended Strobe of READ burst.



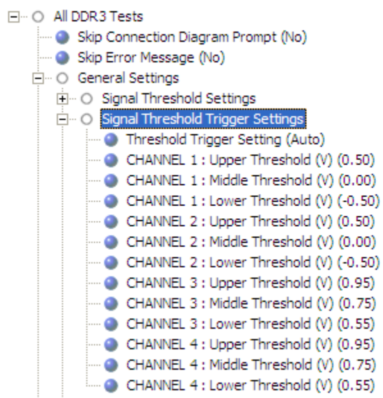
This section will set the threshold settings for Data signal of READ burst and single-ended Strobe of READ burst.



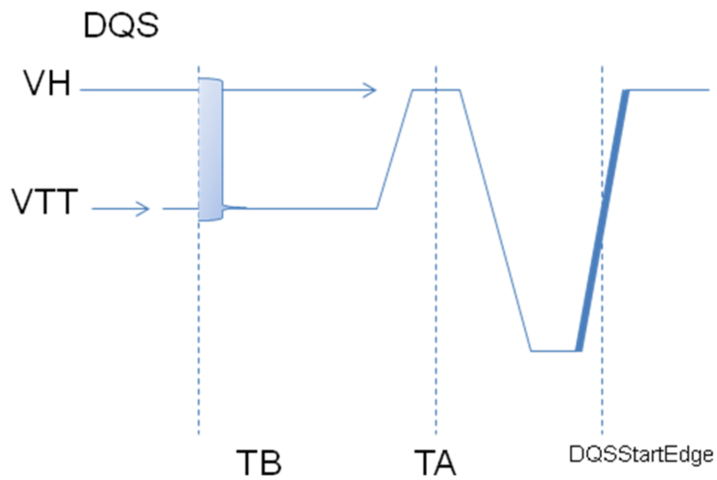
The differential signals will be using +0.5/0/-0.5V for the threshold settings.

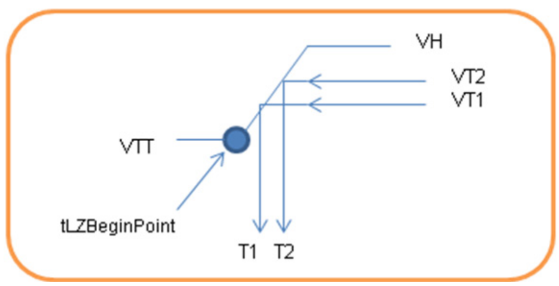


Method 2 Users also have a choice to setup each channel's threshold settings using the following settings.



Finding tLZBeginPoint(DQS) for READ data burst (DDR4)

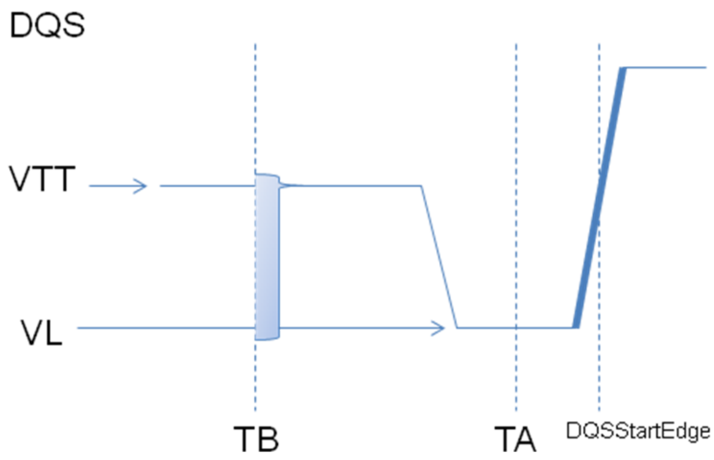


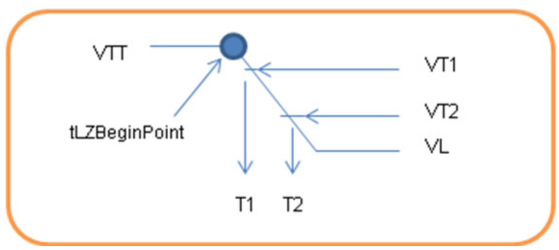


Steps:

1. TA = DQSStartEdge – 1.5 UI
2. TB = DQSStartEdge – 3.0 UI
3. Form a histogram(vert) bounded by TA & TB.
4. VTT = Histogram Min
5. VH = Histogram Max
6. VT1 = VTT+0.3*(VH-VTT)
7. VT2 = VTT+0.6*(VH-VTT)
8. tLZBeginPoint = ((T2 - T1) / (VT2 - VT1)) * (VTT - VT2) + T2;

Finding tLZBeginPoint(DQS) for READ data burst (LPDDR4)

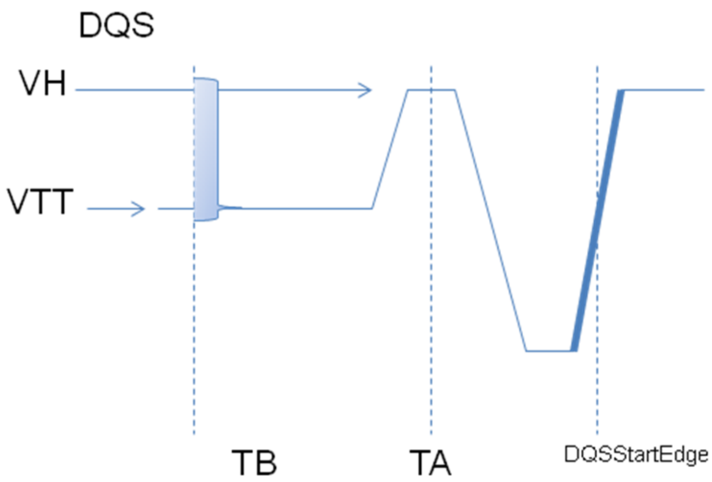


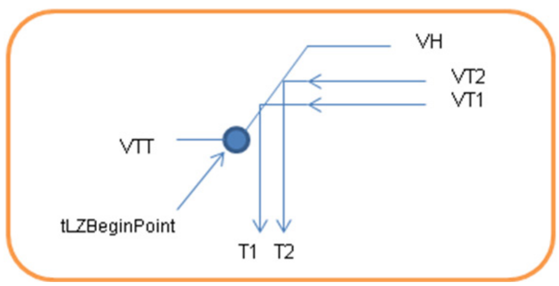


Steps:

1. TA = DQSStartEdge – 0.5 UI
2. TB = DQSStartEdge – 3.0 UI
3. Form a histogram(vert) bounded by TA & TB.
4. VTT = Histogram Max
5. VL = Histogram Min
6. VT1 = VTT-0.3*(VTT-VL)
7. VT2 = VTT-0.6*(VTT-VL)
8. tLZBeginPoint = ((T2 - T1) / (VT2 - VT1)) * (VTT - VT2) + T2;

Finding tLZBeginPoint(DQS) for WRITE data burst

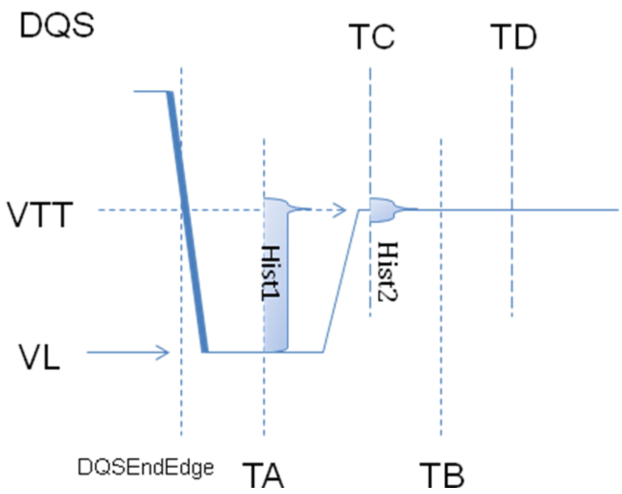


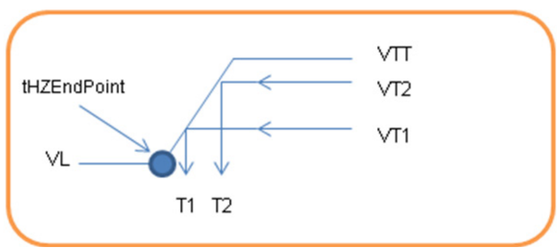


Steps:

1 TA = DQSStartEdge – 1.5 UI
2 TB = DQSStartEdge – 3.0 UI
3 Form a histogram(vert) bounded by TA & TB.
4 VTT = Histogram Min
5 VH = Histogram Max
6 VT1 = VTT+0.3*(VH-VTT)
7 VT2 = VTT+0.6*(VH-VTT)
8 tLZBeginPoint = ((T2 - T1) / (VT2 - VT1)) * (VTT - VT2) + T2;

Finding tHZEndPoint(DQS)

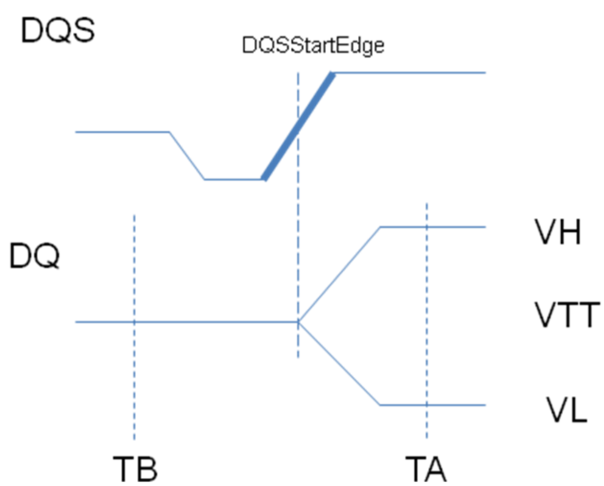


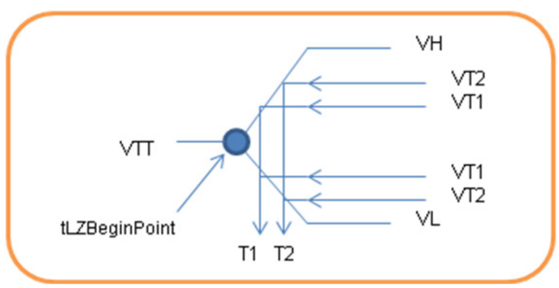


Steps:

1 TA = DQSEndEdge + 0.5 UI
2 TB = DQSEndEdge + 1.0 UI
3 Form a histogram(vert) bounded by TA & TB.
4 VTT = Histogram Max
5 VL = Histogram Min
6 Extra cheking:
   a TC = TB – 0.5 UI
   b TD = TB + 0.5 UI
   c Form Hist2, if Hist2 Mode < VTT, VTT = Hist2 Max
7 VT1 = VL + 0.3*(VTT-VL)
8 VT2 = VL + 0.6*(VTT-VL)
9 tHZEndPoint = ((T2 - T1) / (VT2 - VT1)) * (VL - VT2) + T2;

Finding tLZBeginPoint(DQ)



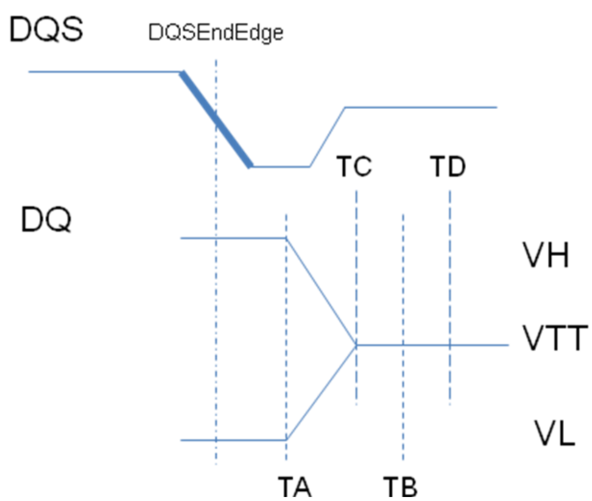


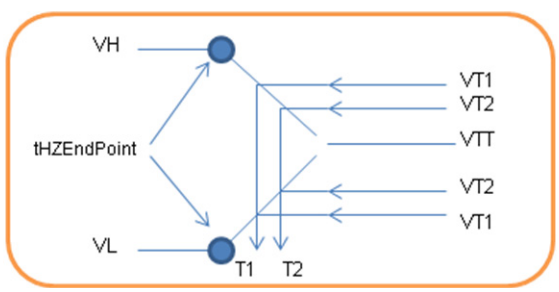
Steps:

1. TA = DQSStartEdge + 0.5 UI
2. TB = DQSStartEdge – 1.0 UI
3. Find VTA, Voltage of DQ at TA
4. Find VTB, Voltage of DQ at TB
5. Form a histogram(vert) bounded by TA & TB.
6. If VTA > VTB,
   - a. VTT = Histogram Min
   - b. VH = Histogram Max
   - c. VT1 = VTT+0.3*(VH-VTT)
   - d. VT2 = VTT+0.6*(VH-VTT)
   - e. tLZBeginPoint = ((T2 - T1) / (VT2 - VT1)) * (VTT - VT2) + T2;

7 If VTB > VTA,
   a VTT = Histogram Max
   b VL = Histogram Min
   c VT1 = VTT-0.3*(VTT-VL)
   d VT2 = VTT-0.6*(VTT-VL)
   e tLZBeginPoint = ((T2 - T1) / (VT2 - VT1)) * (VTT - VT2) + T2;

Find tHZEndPoint(DQ)





Steps:

1 TA = DQSEndEdge + 0.5 UI
2 TB = DQSEndEdge + 1.5 UI
3 TC = TB – 0.5 UI
4 TD = TB + 0.5 UI
5 Find VTA, Voltage of DQ at TA
6 Find VTB, Voltage of DQ at TB

7 Form a histogram(vert) bounded by TA and TB.

8 Form a histogram(vert) bounded by TC and TD.

9 If VTA > VTB,

   a VTT = Histogram(CD) Mode

   b VH = Histogram(AB) Max

   c VT1 = VTT-0.3*(VH-VTT)

   d VT2 = VTT-0.6*(VH-VTT)

   e tHZEndPoint = ((T2 - T1) / (VT2 - VT1)) * (VH - VT2) + T2;

10 If VTB > VTA,

   a VTT = Histogram(CD) Mode

   b VL = Histogram(AB) Min

   c VT1 = VTT+0.3*(VTT-VL)

   d VT2 = VTT+0.6*(VTT-VL)

   e tHZEndPoint = ((T2 - T1) / (VT2 - VT1)) * (VL - VT2) + T2;

Clock Timing (CT)

Clock Period Jitter- tJIT(per)

Rising Edge Measurements

Mode Supported: DDR4, LPDDR4

Signal cycle of interest: READ or WRITE

Require Read/Write separation: No

Signal(s) of Interest:

- Clock Signals

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.

References:

Specifications document	Section#	Table#
DDR4 SDRAM Specification, JESD79-4, September 2012	12	Table 101 and 102
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.1	Table 88

Table 101 — Timing Parameters by Speed Bin for DDR4-1600 to DDR4-2133

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Clock Period Jitter- total	JIT(per)_tot	- 0.1	0.1	- 0.1	0.1	- 0.1	0.1	UI	23

Table 102 — Timing Parameters by Speed Bin for DDR4-2400 to DDR4-3200

Speed		DDR4-2400		DDR4-2666		DDR4-3200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Clock Period Jitter- total	JIT(per)_tot	- 0.1	0.1	- 0.1	0.1	- 0.1	0.1	UI	25

Table 88 — Clock AC Timings

Parameter	Symbol	LPDDR4-1600		LPDDR4-2400		LPDDR4-3200		LPDDR4-4266		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock Timing											
Average clock period	tCK(avg)	1.25	100	0.833	100	0.625	100	0.467	100	ns	
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	TBD	TBD	tCK(avg)	
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	TBD	TBD	tCK(avg)	
Absolute clock period	tCK(abs)	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	ns	
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	TBD	TBD	tCK(avg)	
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	TBD	TBD	tCK(avg)	
Clock period jitter	tJIT(per)	-70	70	-50	50	-40	40	-	TBD	ps	
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	140	-	100	-	80	-	TBD	ps	

Test Overview: The purpose of this test is to measure the difference between a measured clock period and the average clock period across multiple cycles of the clock.

- Clock (Continuous or Burst) — Select either Continuous or Burst to define the Clock Signal.
- Number of Clock Measurements — Set the number of total clock transitions that must be measured. Minimum value that you must set is 200. If you select the Clock as 'Continuous', the memory depth must be set accordingly to capture sufficient number of clock edges. If you select the Clock as 'Burst', the number of clocks set in the burst clock transitions is measured first. You may then repeat as many acquisitions as required to meet the set value.
- Burst Clock Minimum Transition — Option available when you select Clock as Burst. Set the number of clock transitions you may want to test in a given burst. Minimum value that you must set is 202.

Procedure: Example of input period measured:

Clock: Burst, Number of Clock Measurements: 200, Burst Clock Minimum Transition: 202

Example input test signal:

Frequency: 1 kHz, Number of cycles acquired: 202

- The Compliance Test Application:

1. Measures the difference between every period inside a 200 cycle window with the average of the whole window.
2. Calculates the average for periods 1 to 200.

3 Measures the difference between period #1, period #2 and so on up to period #200; with the average and save the resulting value as a measurement result. A total of 200 measurement results are generated.
4 For the next set of measurement values, you must slide the window by one period and the application measures the average of period #2 up to period #201.
5 Compares period #2 with the new average. Continue the comparison for period #3, #4 and so on up to period #201. A total of 200 additional measurement results are generated such that there are 400 measured values overall.
6 For the next set of measurement values, you must slide the window by one more period and the application measures the average of period #3 up to period #202.
7 Compares period #3 with the new average. Continue the comparison for period #4, #5 and so on up to period #202. A total of 200 additional measurement results are generated such that there are 600 measured values overall.
8 When “Burst” is selected for Clock, the process of measurement repeats for as many acquisitions as are required to meet the value set for the “Number of Clock Measurements” parameter, else the test continues to the next step. Note that the time taken for the tests is usually proportional to the value defined for the “Number of Clock Measurements” parameter.
9 From the 600 measured values, check for the smallest and largest values, which are recorded as the worst case values.
10 Compare the worst case values to the compliance test limits.

Expected/Observable Results: The measured value of tJIT(per) shall be within the conformance limits as specified in the JEDEC specification.

Cycle-to-Cycle Period Jitter - tJIT(cc)

Rising Edge Measurements

Mode Supported: DDR4, LPDDR4

Signal cycle of interest: READ or WRITE

Require Read/Write separation: No

Signal(s) of Interest:

- Clock Signals

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.

References:

Specifications document	Section#	Table#
DDR4 SDRAM Specification, JESD79-4, September 2012	12	Table 101 and 102
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.1	Table 88

Table 101 — Timing Parameters by Speed Bin for DDR4-1600 to DDR4-2133

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Cycle to Cycle Period Jitter	tJIT(cc)_total	0.2		0.2		0.2		UI	25

Table 102 — Timing Parameters by Speed Bin for DDR4-2400 to DDR4-3200

Speed		DDR4-2400		DDR4-2666		DDR4-3200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Cycle to Cycle Period Jitter	tJIT(cc)_total	0.2		0.2		0.2		UI	25

Table 88 — Clock AC Timings

Parameter	Symbol	LPDDR4-1600		LPDDR4-2400		LPDDR4-3200		LPDDR4-4266		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock Timing											
Average clock period	tCK(avg)	1.25	100	0.833	100	0.625	100	0.467	100	ns	
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	TBD	TBD	tCK(avg)	
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	TBD	TBD	tCK(avg)	
Absolute clock period	tCK(abs)	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	ns	
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	TBD	TBD	tCK(avg)	
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	TBD	TBD	tCK(avg)	
Clock period jitter	tJIT(per)	-70	70	-50	50	-40	40	-	TBD	ps	
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	140	-	100	-	80	-	TBD	ps	

Test Overview: The purpose of this test is to measure the difference in the clock period between two consecutive clock cycles; that is, the tJIT(cc) Rising Edge Measurement measures the clock period between the consecutive rising edges of a clock cycle.

- Clock (Continuous or Burst) — Select either Continuous or Burst to define the Clock Signal.

- Number of Clock Measurements — Set the number of total clock transitions that must be measured. Minimum value that you must set is 200. If you select the Clock as ‘Continuous’, the memory depth must be set accordingly to capture sufficient number of clock edges. If you select the Clock as ‘Burst’, the number of clocks set in the burst clock transitions is measured first. You may then repeat as many acquisitions as required to meet the set value.
- Burst Clock Minimum Transition — Option available when you select Clock as Burst. Set the number of clock transitions you may want to test in a given burst. Minimum value that you must set is 202.

Procedure: Example of input period measured:

Clock: Burst, Number of Clock Measurements: 200, Burst Clock Minimum Transition: 202

Example input test signal:

Frequency: 1 kHz, Number of cycles acquired: 202

- The Compliance Test Application:

1. Measures the difference between every adjacent pair of periods.
2. Generates a total of 201 measurement results.
3. When “Burst” is selected for Clock, the process of measurement repeats for as many acquisitions as are required to meet the value set for the “Number of Clock Measurements” parameter, else the test continues to the next step. Note that the time taken for the tests is usually proportional to the value defined for the “Number of Clock Measurements” parameter.
4. Once the measurement results are generated, check the results for the smallest and largest values, which are recorded as the worst case values.
5. Compare the worst case values to the compliance test limits.

Expected/Observable Results: The measured value of tJIT(cc) shall be within the conformance limits as specified in the JEDEC specification.

Cumulative Error (across n cycles) - tERR(nper)

Rising Edge Measurements

Mode Supported: DDR4, LPDDR4

Signal cycle of interest: READ or WRITE

Require Read/Write separation: No

Signal(s) of Interest:

- Clock Signals

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.

References: There is no limit found for this test.

Test Overview: The purpose of this test is to measure the difference between a measured clock period and the average clock period across multiple cycles of the clock. Supported measurements include multiple cycle windows with values of “n” (for “n” cycles) where, n is greater than 5 but less than 50.

- Clock (Continuous or Burst) — Select either Continuous or Burst to define the Clock Signal.
- Number of Clock Measurements — Set the number of total clock transitions that must be measured. Minimum value that you must set is 200. If you select the Clock as ‘Continuous’, the memory depth must be set accordingly to capture sufficient number of clock edges. If you select the Clock as ‘Burst’, the number of clocks set in the burst clock transitions is measured first. You may then repeat as many acquisitions as required to meet the set value.
- Burst Clock Minimum Transition — Option available when you select Clock as Burst. Set the number of clock transitions you may want to test in a given burst. Minimum value that you must set is 202.

Procedure: Example of input period measured:

Clock: Burst, Number of Clock Measurements: 200, Burst Clock Minimum Transition: 202

Example input test signal:

Frequency: 1 kHz, Number of cycles acquired: 202

- On the Compliance Test Application:

1. tERR (2per) is very similar to tJIT (per), except that a 2-cycle window is formed inside a large 200-cycle window and the average of the small window is compared against the average of the large window.
2. Calculates the average for periods from 1 to 200.
3. Calculates the average of period #1 and period #2.
4. Calculates the difference of these two averages and the saves the resulting value as a measurement result.
5. Calculates the average of period #2 and period #3 and measures the difference between this average and the average of the large window.
6. Repeats the same procedure up to measuring the average of period #199 and period #200 and comparing this average against the average of the large window. A total of 199 measurement results are generated.
7. For the next set of measurement values, you must slide the large window by one period and the test application repeats the process of calculating the averages and differences. The test application starts by comparing the average of periods 2 and 3 against the average of the new large window (from periods 2

to 201) until it compares the average of periods 200 and 201 with the average of the large window. A total of 199 measurement results are generated, thereby making a total of 398 measurement values overall.

8 For the next set of measurement values, you must slide the large window by one more period and the test application repeats the calculations such that a total of 199 measurement results are generated, thereby making a total of 597 measurement values overall.

9 When "Burst" is selected for Clock, the process of measurement repeats for as many acquisitions as are required to meet the value set for the "Number of Clock Measurements" parameter, else the test continues to the next step. Note that the time taken for the tests is usually proportional to the value defined for the "Number of Clock Measurements" parameter.

10 From the 597 measured values, check for the smallest and largest values, which are recorded as the worst case values.

11 Compare the worst case values to the compliance test limits.

12 tERR(3per) is the same as tERR(2per) except that the small window size is three periods wide. tERR(4per) uses a small window size of four periods and tERR(5per) uses five periods.

13 tERR(6-10per) runs tERR(6per), tERR(7per), tERR(8per), tERR(9per) and tERR(10per). The test application combines all the measurement results together into one big pool and checks for the smallest and largest values.

14 tERR(11-50per) does the same for tERR(11per) through tERR(50per).

Expected/Observable Results: The measured values of tERR shall meet the user defined limits.

Average High Pulse Width - tCH(avg)

Mode Supported: DDR4, LPDDR4

Signal cycle of interest: READ or WRITE

Require Read/Write separation: No

Signal(s) of Interest:

- Clock Signals

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.

References:

Specifications document	Section#	Table#
DDR4 SDRAM Specification, JESD79-4, September 2012	12	Table 101 and 102
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.1	Table 88

Table 101 — Timing Parameters by Speed Bin for DDR4-1600 to DDR4-2133

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	

Table 102 — Timing Parameters by Speed Bin for DDR4-2400 to DDR4-3200

Speed		DDR4-2400		DDR4-2666		DDR4-3200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	

Table 88 — Clock AC Timings

Parameter	Symbol	LPDDR4-1600		LPDDR4-2400		LPDDR4-3200		LPDDR4-4266		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock Timing											
Average clock period	tCK(avg)	1.25	100	0.833	100	0.625	100	0.467	100	ns	
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	TBD	TBD	tCK(avg)	
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	TBD	TBD	tCK(avg)	
Absolute clock period	tCK(abs)	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	ns	
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	TBD	TBD	tCK(avg)	
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	TBD	TBD	tCK(avg)	
Clock period jitter	tJIT(per)	-70	70	-50	50	-40	40	-	TBD	ps	
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	140	-	100	-	80	-	TBD	ps	

Test Overview: The purpose of this test is to measure the average duty cycle of all positive pulse widths within a window of 200 consecutive cycles.

- Clock (Continuous or Burst) — Select either Continuous or Burst to define the Clock Signal.

- Number of Clock Measurements — Set the number of total clock transitions that must be measured. Minimum value that you must set is 200. If you select the Clock as ‘Continuous’, the memory depth must be set accordingly to capture sufficient number of clock edges. If you select the Clock as ‘Burst’, the number of clocks set in the burst clock transitions is measured first. You may then repeat as many acquisitions as required to meet the set value.
- Burst Clock Minimum Transition — Option available when you select Clock as Burst. Set the number of clock transitions you may want to test in a given burst. Minimum value that you must set is 202.

Procedure: Example of input period measured:

Clock: Burst, Number of Clock Measurements: 200, Burst Clock Minimum Transition: 202

Example input test signal:

Frequency: 1 kHz, Number of cycles acquired: 202

- The Compliance Test Application:

1. Measures a sliding “window” of 200 cycles.
2. Measures the width of the high pulses from cycle #1 to cycle #200 and determines the average value for this window; thereby, generating one measurement result.
3. Measures the width of the high pulses from cycle #2 to cycle #201 and determines the average value for this window; thereby, generating one more measurement result and two measurement values overall.
4. Measures the width of the high pulses from cycle #3 to cycle #202 and determines the average value for this window; thereby, generating one more measurement result and three measurement results overall.
5. When “Burst” is selected for Clock, the process of measurement repeats for as many acquisitions as are required to meet the value set for the “Number of Clock Measurements” parameter, else the test continues to the next step. Note that the time taken for the tests is usually proportional to the value defined for the “Number of Clock Measurements” parameter.
6. From the three measured values, check for the smallest and largest values, which are recorded as the worst case values.
7. Compare the worst case values to the compliance test limits.

Expected/Observable Results: The measured value of tCH shall be within the conformance limits as specified in the JEDEC specification.

Absolute High Pulse Width - tCH(abs)

Mode Supported: LPDDR4

Signal cycle of interest: READ or WRITE

Require Read/Write separation: No

Signal(s) of Interest:
- Clock Signals

Required Signals: Needed to perform this test on oscilloscope:
- Pin Under Test, PUT = any of the signal of interest defined above.

References:

Specifications document	Section#	Table#
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.1	Table 88

Table 88 — Clock AC Timings

Parameter	Symbol	LPDDR4-1600		LPDDR4-2400		LPDDR4-3200		LPDDR4-4266		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock Timing											
Average clock period	tCK(avg)	1.25	100	0.833	100	0.625	100	0.467	100	ns	
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	TBD	TBD	tCK(avg)	
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	TBD	TBD	tCK(avg)	
Absolute clock period	tCK(abs)	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	ns	
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	TBD	TBD	tCK(avg)	
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	TBD	TBD	tCK(avg)	
Clock period jitter	tJIT(per)	-70	70	-50	50	-40	40	-	TBD	ps	
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	140	-	100	-	80	-	TBD	ps	

Test Overview: The purpose of this test is to measure the average duty cycle of all positive pulse widths within a window of 200 consecutive cycles.

- Clock (Continuous or Burst) — Select either Continuous or Burst to define the Clock Signal.
- Number of Clock Measurements — Set the number of total clock transitions that must be measured. Minimum value that you must set is 200. If you select the Clock as ‘Continuous’, the memory depth must be set accordingly to capture sufficient number of clock edges. If you select the Clock as ‘Burst’, the number of clocks set in the burst clock transitions is measured first. You may then repeat as many acquisitions as required to meet the set value.

- Burst Clock Minimum Transition — Option available when you select Clock as Burst. Set the number of clock transitions you may want to test in a given burst. Minimum value that you must set is 202.

Procedure: Example of input period measured:

Clock: Burst, Number of Clock Measurements: 200, Burst Clock Minimum Transition: 202

Example input test signal:

Frequency: 1 kHz, Number of cycles acquired: 202

- The Compliance Test Application:

1 Measures a sliding “window” of 200 cycles.
2 Measures the width of the high pulses from cycle #1 to cycle #200 and determines the average value for this window; thereby, generating one measurement result.
3 Measures the width of the high pulses from cycle #2 to cycle #201 and determines the average value for this window; thereby, generating one more measurement result and two measurement values overall.
4 Measures the width of the high pulses from cycle #3 to cycle #202 and determines the average value for this window; thereby, generating one more measurement result and three measurement results overall.
5 When “Burst” is selected for Clock, the process of measurement repeats for as many acquisitions as are required to meet the value set for the “Number of Clock Measurements” parameter, else the test continues to the next step. Note that the time taken for the tests is usually proportional to the value defined for the “Number of Clock Measurements” parameter.
6 From the three measured values, check for the smallest and largest values, which are recorded as the worst case values.
7 Compare the worst case values to the compliance test limits.

Expected/Observable Results: The measured value of tCH(abs) shall be within the conformance limits as specified in the JEDEC specification.

Average Low Pulse Width - tCL(avg)

Mode Supported: DDR4, LPDDR4

Signal cycle of interest: READ or WRITE

Require Read/Write separation: No

Signal(s) of Interest:

- Clock Signals

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.

References:

Specifications document	Section#	Table#
DDR4 SDRAM Specification, JESD79-4, September 2012	12	Table 101 and 102
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.1	Table 88

Table 101 — Timing Parameters by Speed Bin for DDR4-1600 to DDR4-2133

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	

Table 102 — Timing Parameters by Speed Bin for DDR4-2400 to DDR4-3200

Speed		DDR4-2400		DDR4-2666		DDR4-3200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	

Table 88 — Clock AC Timings

Parameter	Symbol	LPDDR4-1600		LPDDR4-2400		LPDDR4-3200		LPDDR4-4266		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock Timing											
Average clock period	tCK(avg)	1.25	100	0.833	100	0.625	100	0.467	100	ns	
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	TBD	TBD	tCK(avg)	
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	TBD	TBD	tCK(avg)	
Absolute clock period	tCK(abs)	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	ns	
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	TBD	TBD	tCK(avg)	
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	TBD	TBD	tCK(avg)	
Clock period jitter	tJIT(per)	-70	70	-50	50	-40	40	-	TBD	ps	
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	140	-	100	-	80	-	TBD	ps	

Test Overview: The purpose of this test is to measure the average duty cycle of all negative pulse widths within a window of 200 consecutive cycles.

- Clock (Continuous or Burst) — Select either Continuous or Burst to define the Clock Signal.

- Number of Clock Measurements — Set the number of total clock transitions that must be measured. Minimum value that you must set is 200. If you select the Clock as 'Continuous', the memory depth must be set accordingly to capture sufficient number of clock edges. If you select the Clock as 'Burst', the number of clocks set in the burst clock transitions is measured first. You may then repeat as many acquisitions as required to meet the set value.
- Burst Clock Minimum Transition — Option available when you select Clock as Burst. Set the number of clock transitions you may want to test in a given burst. Minimum value that you must set is 202.

Procedure: Example of input period measured:

Clock: Burst, Number of Clock Measurements: 200, Burst Clock Minimum Transition: 202

Example input test signal:

Frequency: 1 kHz, Number of cycles acquired: 202

- The Compliance Test Application:

1. Measures a sliding "window" of 200 cycles.
2. Measures the width of the high pulses from cycle #1 to cycle #200 and determines the average value for this window; thereby, generating one measurement result.
3. Measures the width of the high pulses from cycle #2 to cycle #201 and determines the average value for this window; thereby, generating one more measurement result and two measurement values overall.
4. Measures the width of the high pulses from cycle #3 to cycle #202 and determines the average value for this window; thereby, generating one more measurement result and three measurement results overall.
5. When "Burst" is selected for Clock, the process of measurement repeats for as many acquisitions as are required to meet the value set for the "Number of Clock Measurements" parameter, else the test continues to the next step. Note that the time taken for the tests is usually proportional to the value defined for the "Number of Clock Measurements" parameter.
6. From the three measured values, check for the smallest and largest values, which are recorded as the worst case values.
7. Compare the worst case values to the compliance test limits.

Expected/Observable Results: The measured value of tCL(avg) shall be within the conformance limits as specified in the JEDEC specification.

Absolute Low Pulse Width - tCL(abs)

Mode Supported: LPDDR4

Signal cycle of interest: READ or WRITE

Require Read/Write separation: No

Signal(s) of Interest:

- Clock Signals

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.

References:

Specifications document	Section#	Table#
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.1	Table 88

Table 88 — Clock AC Timings

Parameter	Symbol	LPDDR4-1600		LPDDR4-2400		LPDDR4-3200		LPDDR4-4266		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock Timing											
Average clock period	tCK(avg)	1.25	100	0.833	100	0.625	100	0.467	100	ns	
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	TBD	TBD	tCK(avg)	
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	TBD	TBD	tCK(avg)	
Absolute clock period	tCK(abs)	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	ns	
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	TBD	TBD	tCK(avg)	
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	TBD	TBD	tCK(avg)	
Clock period jitter	tJIT(per)	-70	70	-50	50	-40	40	-	TBD	ps	
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	140	-	100	-	80	-	TBD	ps	

Test Overview: The purpose of this test is to measure the average duty cycle of all negative pulse widths within a window of 200 consecutive cycles.

- Clock (Continuous or Burst) — Select either Continuous or Burst to define the Clock Signal.
- Number of Clock Measurements — Set the number of total clock transitions that must be measured. Minimum value that you must set is 200. If you select the Clock as ‘Continuous’, the memory depth must be set accordingly to capture sufficient number of clock edges. If you select the Clock as ‘Burst’, the number of clocks set in the burst clock transitions is measured first. You may then repeat as many acquisitions as required to meet the set value.

- Burst Clock Minimum Transition — Option available when you select Clock as Burst. Set the number of clock transitions you may want to test in a given burst. Minimum value that you must set is 202.

Procedure: Example of input period measured:

Clock: Burst, Number of Clock Measurements: 200, Burst Clock Minimum Transition: 202

Example input test signal:

Frequency: 1 kHz, Number of cycles acquired: 202

- The Compliance Test Application:

1. Measures a sliding “window” of 200 cycles.
2. Measures the width of the high pulses from cycle #1 to cycle #200 and determines the average value for this window; thereby, generating one measurement result.
3. Measures the width of the high pulses from cycle #2 to cycle #201 and determines the average value for this window; thereby, generating one more measurement result and two measurement values overall.
4. Measures the width of the high pulses from cycle #3 to cycle #202 and determines the average value for this window; thereby, generating one more measurement result and three measurement results overall.
5. When “Burst” is selected for Clock, the process of measurement repeats for as many acquisitions as are required to meet the value set for the “Number of Clock Measurements” parameter, else the test continues to the next step. Note that the time taken for the tests is usually proportional to the value defined for the “Number of Clock Measurements” parameter.
6. From the three measured values, check for the smallest and largest values, which are recorded as the worst case values.
7. Compare the worst case values to the compliance test limits.

Expected/Observable Results: The measured value of tCL(abs) shall be within the conformance limits as specified in the JEDEC specification.

Half Period Jitter - tJIT(duty)

Jitter Average High - tJIT(duty-high)

Jitter Average Low - tJIT(duty-low)

Mode Supported: DDR4, LPDDR4

Signal cycle of interest: READ or WRITE

Require Read/Write separation: No

Signal(s) of Interest:

- Clock Signals

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.

References: There is no limit found for this test.

Test Overview: The tJIT(duty) can be divided into tJIT(CH) and tJIT(LH).

The tJIT(CH) Jitter Average High Measurement test measures the time period between a positive pulse width of a cycle in the waveform and the average positive pulse width of all cycles in a 200 consecutive cycle window.

The tJIT(LH) Jitter Average Low Measurement test measures the time period between a negative pulse width of a cycle in the waveform and the average negative pulse width of all cycles in a 200 consecutive cycle window.

- Clock (Continuous or Burst) — Select either Continuous or Burst to define the Clock Signal.
- Number of Clock Measurements — Set the number of total clock transitions that must be measured. Minimum value that you must set is 200. If you select the Clock as ‘Continuous’, the memory depth must be set accordingly to capture sufficient number of clock edges. If you select the Clock as ‘Burst’, the number of clocks set in the burst clock transitions is measured first. You may then repeat as many acquisitions as required to meet the set value.
- Burst Clock Minimum Transition — Option available when you select Clock as Burst. Set the number of clock transitions you may want to test in a given burst. Minimum value that you must set is 202.

Procedure: Example of input period measured:

Clock: Burst, Number of Clock Measurements: 200, Burst Clock Minimum Transition: 202

Example input test signal:

Frequency: 1 kHz, Number of cycles acquired: 202

- For tJIT(CH) measurement, the Compliance Test Application:

1. Measures the difference between every high pulse width inside a 200 cycle window with the average of the whole window.
2. Calculates the average for high pulse width from 1 to 200.
3. Measures the difference between high pulse width #1, high pulse width #2 and so on up to high pulse width #200; with the average and saves the resulting value as a measurement result. A total of 200 measurement results are generated.

4 For the next set of measurement values, you must slide the window by one period and the application measures the average of high pulse width #2 up to high pulse width #201.
5 Compares high pulse width #2 with the new average. Continue the comparison for high pulse width #3, #4 and so on up to high pulse width #201. A total of 200 additional measurement results are generated such that there are 400 measured values overall.
6 For the next set of measurement values, you must slide the window by one more period and the application measures the average of high pulse width #3 up to high pulse width #202.
7 Compares high pulse width #3 with the new average. Continue the comparison for high pulse width #4, #5 and so on up to high pulse width #202. A total of 200 additional measurement results are generated such that there are 600 measured values overall.
8 When “Burst” is selected for Clock, the process of measurement repeats for as many acquisitions as are required to meet the value set for the “Number of Clock Measurements” parameter, else the test continues to the next step. Note that the time taken for the tests is usually proportional to the value defined for the “Number of Clock Measurements” parameter.
9 From the 600 measured values, check for the smallest and largest values, which are recorded as the worst case values.
10 Compare the worst case values to the compliance test limits.

For tJIT(CH) measurement, the Compliance Test Application:

1. Repeats the procedural steps as described above for the measurement of tJIT(CH) using low pulse widths for testing comparison instead of using high pulse widths.
2. From the 600 measured values, check for the smallest and largest values, which are recorded as the worst case values.
3. Compare the worst case values to the compliance test limits.

Expected/Observable Results: The measured value of tJIT(duty) shall meet the user defined limits.

Average Clock Period - tCK(avg)

Rising Edge Measurements

Mode Supported: DDR4, LPDDR4

Signal cycle of interest: READ or WRITE

Require Read/Write separation: No

Signal(s) of Interest:

- Clock Signals

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.

References:

Specifications document	Section#	Table#
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.1	Table 88

Table 88 — Clock AC Timings

Parameter	Symbol	LPDDR4-1600		LPDDR4-2400		LPDDR4-3200		LPDDR4-4266		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock Timing											
Average clock period	tCK(avg)	1.25	100	0.833	100	0.625	100	0.467	100	ns	
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	TBD	TBD	tCK(avg)	
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	TBD	TBD	tCK(avg)	
Absolute clock period	tCK(abs)	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	ns	
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	TBD	TBD	tCK(avg)	
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	TBD	TBD	tCK(avg)	
Clock period jitter	tJIT(per)	-70	70	-50	50	-40	40	-	TBD	ps	
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	140	-	100	-	80	-	TBD	ps	

Test Overview: tCK(avg) is the average clock period within a 200 consecutive cycle window. The tCK(avg) Rising Edge Measurement measures the average time period between consecutive rising edges of a cycle within the waveform window.

- Clock (Continuous or Burst) — Select either Continuous or Burst to define the Clock Signal.
- Number of Clock Measurements — Set the number of total clock transitions that must be measured. Minimum value that you must set is 200. If you select the Clock as 'Continuous', the memory depth must be set accordingly to capture sufficient number of clock edges. If you select the Clock as 'Burst', the number of clocks set in the burst clock transitions is measured first. You may then repeat as many acquisitions as required to meet the set value.
- Burst Clock Minimum Transition — Option available when you select Clock as Burst. Set the number of clock transitions you may want to test in a given burst. Minimum value that you must set is 202.

Procedure: Example of input period measured:

Clock: Burst, Number of Clock Measurements: 200, Burst Clock Minimum Transition: 202

Example input test signal:

Frequency: 1 kHz, Number of cycles acquired: 202

- The Compliance Test Application:

1 Measures a sliding “window” of 200 cycles.
2 Measures the width of the high pulses from cycle #1 to cycle #200 and determines the average value for this window; thereby, generating one measurement result.
3 Measures the width of the high pulses from cycle #2 to cycle #201 and determines the average value for this window; thereby, generating one more measurement result and two measurement values overall.
4 Measures the width of the high pulses from cycle #3 to cycle #202 and determines the average value for this window; thereby, generating one more measurement result and three measurement results overall.
5 When “Burst” is selected for Clock, the process of measurement repeats for as many acquisitions as are required to meet the value set for the “Number of Clock Measurements” parameter, else the test continues to the next step. Note that the time taken for the tests is usually proportional to the value defined for the “Number of Clock Measurements” parameter.
6 From the three measured values, check for the smallest and largest values, which are recorded as the worst case values.
7 Compare the worst case values to the compliance test limits.

Expected/Observable Results: The measured value of tCK(avg) shall meet the user defined limits.

Absolute Clock Period - tCK(abs)

Rising Edge Measurements

Mode Supported: LPDDR4

Signal cycle of interest: READ or WRITE

Require Read/Write separation: No

Signal(s) of Interest:

- Clock Signals

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.

References:

Specifications document	Section#	Table#
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.1	Table 88

Table 88 — Clock AC Timings

Parameter	Symbol	LPDDR4-1600		LPDDR4-2400		LPDDR4-3200		LPDDR4-4266		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock Timing											
Average clock period	tCK(avg)	1.25	100	0.833	100	0.625	100	0.467	100	ns	
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	TBD	TBD	tCK(avg)	
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	TBD	TBD	tCK(avg)	
Absolute clock period	tCK(abs)	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	ns	
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	TBD	TBD	tCK(avg)	
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	TBD	TBD	tCK(avg)	
Clock period jitter	tJIT(per)	-70	70	-50	50	-40	40	-	TBD	ps	
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	140	-	100	-	80	-	TBD	ps	

Test Overview: tCK(abs) is the absolute clock period within a 200 consecutive cycle window. The tCK(abs) Rising Edge Measurement measures the absolute time period between consecutive rising edges of a cycle within the waveform window.

- Clock (Continuous or Burst) — Select either Continuous or Burst to define the Clock Signal.
- Number of Clock Measurements — Set the number of total clock transitions that must be measured. Minimum value that you must set is 200. If you select the Clock as 'Continuous', the memory depth must be set accordingly to capture sufficient number of clock edges. If you select the Clock as 'Burst', the number of clocks set in the burst clock transitions is measured first. You may then repeat as many acquisitions as required to meet the set value.
- Burst Clock Minimum Transition — Option available when you select Clock as Burst. Set the number of clock transitions you may want to test in a given burst. Minimum value that you must set is 202.

Procedure: Example of input period measured:

Clock: Burst, Number of Clock Measurements: 200, Burst Clock Minimum Transition: 202

Example input test signal:

Frequency: 1 kHz, Number of cycles acquired: 202

- The Compliance Test Application:

1 Measures a sliding “window” of 200 cycles.
2 Measures the width of the high pulses from cycle #1 to cycle #200 and determines the average value for this window; thereby, generating one measurement result.
3 Measures the width of the high pulses from cycle #2 to cycle #201 and determines the average value for this window; thereby, generating one more measurement result and two measurement values overall.
4 Measures the width of the high pulses from cycle #3 to cycle #202 and determines the average value for this window; thereby, generating one more measurement result and three measurement results overall.
5 When “Burst” is selected for Clock, the process of measurement repeats for as many acquisitions as are required to meet the value set for the “Number of Clock Measurements” parameter, else the test continues to the next step. Note that the time taken for the tests is usually proportional to the value defined for the “Number of Clock Measurements” parameter.
6 From the three measured values, check for the smallest and largest values, which are recorded as the worst case values.
7 Compare the worst case values to the compliance test limits.

Expected/Observable Results: The measured value of tCK(abs) shall meet the user defined limits.

Data Strobe Timing (DST)

tWPRE Test – Write preamble

Mode Supported: DDR4 , LPDDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:
- Data Strobe Signal (supported by Data Signal)

Optional Signal(s):
- Chip Select Signal (this signal is used to separate DQS signals from different rank of memory).

Required Signals: Needed to perform this test on oscilloscope:
- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (* Optional)

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the time when DQS start driving high (*preamble behavior) to the first DQS signal rising edge crossing for write cycle. The limit is definable by the customers for their evaluation tests usage.

Procedure:
1. Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)
2. Take the first valid WRITE burst found.
3. Find tLZBeginPoint of the said burst. (See notes on "Finding tLZBeginPoint(DQS) for WRITE data burst" on page 74)
4. Find the first rising edge on DQS of the found burst.
5. tWPRE is the time interval of the found rising DQS edge to the tLZBeginPoint found.
6. Report tWPRE.

Expected/Observable Results: The measured tWPRE shall meet the user defined limit.

tWPST Test – Write postamble

Mode Supported: DDR4 , LPDDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:
- Data Strobe Signal (supported by Data Signal)

Optional Signal(s):
- Chip Select Signal (this signal is used to separate DQS signals from different rank of memory).

Required Signals: Needed to perform this test on oscilloscope:
- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (* Optional)

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the time when DQS no longer driving (from High/Low state to Hi-Impedance) from the last DQS signal crossing(last bit of the write data burst) for Write Cycle. The limit is definable by the customers for their evaluation tests usage.

Procedure:
1. Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)
2. Take the first valid WRITE burst found.
3. Find tHZEndPoint of the said burst. (See notes on "Finding tHZEndPoint(DQS)" on page 75)
4. Find the last falling edge on DQS prior to tHZEndPoint found.
5. tWPST is the time interval of the found falling DQS edge's crossing to the tHZEndPoint found.
6. Report tWPST.

Expected/Observable Results: The measured tWPST shall meet the user defined limit.

tDQSS Test – DQS latching transition to associated clock edge

Mode Supported: DDR4 , LPDDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:
- Data Strobe Signal (supported by Data Signal)
- Clock Signal

Optional Signal(s):
- Chip Select Signal (this signal is used to separate DQS signals from different rank of memory).

Required Signals: Needed to perform this test on oscilloscope:
- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal
- Chip Select Signal, CS (* Optional)

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the time interval from data strobe output (DQS rising Edge) access time to the associated clock (crossing point). The limit is definable by the customers for their evaluation tests usage.

Procedure:
1. Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)
2. Take the first valid WRITE burst found.
3. Find all valid rising DQS crossings in the said burst. (See notes on "Threshold Settings" on page 69)
4. For all DQS crossings found, locate the nearest Clock rising crossing. (See notes on "Threshold Settings" on page 69).
5. Take the time different from DQS crossing to Clock crossing found as the tDQSS.
6. Determine the worst result from the set of tDQSS measured.

Expected/Observable Results: The worst measured tDQSS shall meet the user defined limit.

tDQSH Test – DQS input high pulse width

Mode Supported: DDR4 , LPDDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:
- Data Strobe Signal (supported by Data Signal)

Optional Signal(s):
- Chip Select Signal (this signal is used to separate DQS signals from different rank of memory).

Required Signals: Needed to perform this test on oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (* Optional)

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the width of the high level of Data Strobe signal. The limit is definable by the customers for their evaluation tests usage.

Procedure:

1 Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)

2 Take the first valid WRITE burst found.

3 Find all valid rising and falling DQS crossings in the said burst. (See notes on "Threshold Settings" on page 69)

4 tDQSH is time started from a rising edge of the DQS and ended at the following falling edge.

5 Collect all tDQSH.

6 Determine the worst result from the set of tDQSH measured.

Expected/Observable Results: The worst measured tDQSH shall meet the user defined limit.

tDQSL Test – DQS input low pulse width

Mode Supported: DDR4 , LPDDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Optional Signal(s):

- Chip Select Signal (this signal is used to separate DQS signals from different rank of memory).

Required Signals: Needed to perform this test on oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (* Optional)

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the width of the low level of clock signal. The limit is definable by the customers for their evaluation tests usage.

Procedure:

1 Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)

2 Take the first valid WRITE burst found.

3 Find all valid rising and falling DQS crossings in the said burst. (See notes on "Threshold Settings" on page 69)

4 tDQSL is time started from a falling edge of the DQS and ended at the following rising edge.

5 Collect all tDQSL.

6 Determine the worst result from the set of tDQSL measured.

Expected/Observable Results: The worst measured tDQSL shall meet the user defined limit.

tRPRE Test – Read preamble

Mode Supported: DDR4 , LPDDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Optional Signal(s):

- Chip Select Signal (this signal is used to separate DQS signals from different rank of memory).

Required Signals: Needed to perform this test on oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (* Optional)

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the time when DQS start driving low (*preamble behavior) to the first DQS signal crossing for Read Cycle. The limit is definable by the customers for their evaluation tests usage.

Procedure:

1 Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)

2 Take the first valid READ burst found.

3 Find tLZBeginPoint of the said burst. (See notes on "Finding tLZBeginPoint(DQS) for READ data burst (DDR4)" on page 72 or "Finding tLZBeginPoint(DQS) for READ data burst (LPDDR4)" on page 73)

4 Find the first rising edge on DQS of the found burst.

5 tRPRE is the time interval of the found rising DQS edge to the tLZBeginPoint found.

6 Report tRPRE.

Expected/Observable Results: The measured tRPRE shall meet the user defined limit.

tRPST Test – Read postamble

Mode Supported: DDR4 , LPDDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Optional Signal(s):

- Chip Select Signal (this signal is used to separate DQS signals from different rank of memory).

Required Signals: Needed to perform this test on oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (* Optional)

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the time when DQS no longer driving (from High/Low state to Hi-Impedance) from the last DQS signal crossing (last bit of the read data burst) for Read Cycle. The limit is definable by the customers for their evaluation tests usage.

Procedure:

1 Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)

2 Take the first valid READ burst found.

3 Find tHZEndPoint of the said burst. (See notes on "Finding tHZEndPoint(DQS)" on page 75)

4 Find the last falling edge on DQS prior to tHZEndPoint found.

5 tRPST is the time interval of the found falling DQS edge's crossing to the tHZEndPoint found.

6 Report tRPST.

Expected/Observable Results: The measured tRPST shall meet the user defined limit.

tDQSCK Test – DQS output access time from CK,/CK

Mode Supported: DDR4 , LPDDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)
- Clock Signal (CK as Reference Signal)

Optional Signal(s):

- Chip Select Signal (this signal is used to separate DQS signals from different rank of memory)

Required Signals: Needed to perform this test on oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (* Optional)

References:

Specifications document	Section#	Table#
LPDDR4 SDRAM Specification, JESD209-4, August 2014	4.6	Table 16

Table 16 — tDQSCK Timing Table

Parameter	Symbol	Min	Max	Unit	Notes
DQS Output Access Time from CK_t/CK_c	tDQSCK	1.5	3.5	ns	1
DQS Output Access Time from CK_t/CK_c - Temperature Variation	tDQSCK_temp	-	4	ps/°C	2
DQS Output Access Time from CK_t/CK_c - Voltage Variation	tDQSCK_volt	-	7	ps/mV	3

NOTE 1 Includes DRAM process, voltage and temperature variation. It includes the AC noise impact for frequencies > 20 MHz and max voltage of 45 mV pk-pk from DC-20 MHz at a fixed temperature on the package. The volage supply noise must comply to the component Min-Max DC Operating conditions.

NOTE 2 tDQSCK_temp max delay variation as a function of Temperature.

NOTE 3 tDQSCK_volt max delay variation as a function of DC voltage variation for VDDQ and VDD2. tDQSCK_volt should be used to calculate timing variation due to VDDQ and VDD2 noise < 20 MHz. Host controller do not need to account for any variation due to VDDQ and VDD2 noise > 20 MHz. The voltage supply noise must comply to the component Min-Max DC Operating conditions. The voltage variation is defined as the Max[abs{tDQSCKmin@V1-tDQSCKmax@V2}, abs{tDQSCKmax@V1-tDQSCKmin@V2}]/abs{V1-V2}. For tester measurement VDDQ = VDD2 is assumed.

Test Overview: The purpose of this test is to verify the time interval from data strobe output(DQS Rising Edge) access time to the nearest rising/falling edge of the clock. The limit is definable by the customers for their evaluation tests usage.

Procedure:

1. Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)
2. Take the first valid READ burst found.
3. Find all valid rising DQS crossings at V_{REF} in the said burst. (See notes on "Threshold Settings" on page 69)
4. For all DQS crossings found, locate the nearest rising Clock crossing at 0V. (See notes on "Threshold Settings" on page 69)
5. Take the time different from DQS crossing to the corresponding Clock crossing as the tDQSCK.
6. Determine the worst result from the set of tDQSCK measured.

Expected/Observable Results: The worst measured tDQSCK shall meet the user defined limit.

tDVAC(Clock) Test – Time above $V_{IHdiff\ (AC)}$/ below $V_{ILdiff\ (AC)}$

Mode Supported: DDR4

Signal cycle of interest: READ or WRITE

Require Read/Write separation: No

Signal(s) of Interest:

- Clock Signals

Required Signals: Needed to perform this test on oscilloscope:

- Clock Signal, CK

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the time of clock signal above $V_{IHdiff\ (AC)}$ and below $V_{ILdiff\ (AC)}$. The limit is definable by the customers for their evaluation tests usage.

Procedure:

1. Pre-condition the oscilloscope.
2. Trigger on the rising edge of the clock signal under test.
3. Find all crossings on rising/falling edge of the signal under test that cross $V_{ILdiff\ (AC)}$.
4. Find all crossings on rising/falling edge of the signal under test that cross $V_{IHdiff\ (AC)}$.
5. tVAC(Clock) is time started from a rising $V_{IHdiff\ (AC)}$ cross point and ended at the following falling $V_{IHdiff\ (AC)}$ cross point.
6. tVAC(Clock) is also the time started from a falling $V_{ILdiff\ (AC)}$ cross point and ended at the following rising $V_{ILdiff\ (AC)}$ cross point.
7. Collect all tVAC(Clock).
8. Determine the worst result from the set of tVAC(Clock) measured.
9. Report the value of worst tDVAC(Clock). No compliance limit checking performed for this test.

Expected/Observable Results: The worst measured tVAC(Clock) shall meet the user defined limit.

tLZ(DQS) Test – DQS low-impedance time from CK,/CK

Mode Supported: DDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)
- Clock Signal (CK as Reference Signal)

Optional Signal(s):

- Chip Select Signal (this signal is used to separate DQS signals from different rank of memory)

Required Signals: Needed to perform this test on oscilloscope:

- Data Signal, DQ

- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (* Optional)

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the time when DQS start driving(*from tristate to High/Low state) to the clock signal crossing. The limit is definable by the customers for their evaluation tests usage.

Procedure:

1. Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)
2. Take the first valid READ burst found.
3. Find tLZBeginPoint of the said burst. (See notes on "Finding tLZBeginPoint(DQS) for READ data burst (DDR4)" on page 72 or "Finding tLZBeginPoint(DQS) for READ data burst (LPDDR4)" on page 73)
4. Find the nearest Clock rising edge.
5. tLZ(DQS) is the time interval of the found Clock rising edge's crossing point to the tLZBeginPoint found.
6. Report tLZ(DQS).

Expected/Observable Results: The measured tLZ(DQS) shall meet the user defined limit.

tHZ(DQS) Test – DQS high-Z from clock

Mode Supported: DDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)
- Clock Signal (CK as Reference Signal)

Optional Signal(s):

- Chip Select Signal (this signal is used to separate DQS signals from different rank of memory)

Required Signals: Needed to perform this test on oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (* Optional)

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the time when DQS no longer driving (*from Low state to the High-impedance state) to the reference clock signal crossing. The limit is definable by the customers for their evaluation tests usage.

Procedure:

1. Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)
2. Take the first valid READ burst found.
3. Find Strobe tHZ end point of the said burst. (See notes on "Finding tHZEndPoint(DQS)" on page 75)
4. Find the nearest Clock rising crossing.
5. tHZ(DQS) is the time interval of the found Clock rising edge's crossing point to the tHZ end point found.
6. Report tHZ(DQS).

Expected/Observable Results: The measured tHZ(DQS) shall meet the user defined limit.

tQSH Test – DQS Output High Pulse Width

Mode Supported: DDR4 , LPDDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Optional Signal(s):

- Chip Select Signal (this signal is used to separate DQS signals from different rank of memory).

Required Signals: Needed to perform this test on oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (* Optional)

References:

Specifications document	Section#	Table#
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.5	Table 92

Table 92 — Read output timings (cont'd)

Parameter	Symbol	LPDDR4-1600/1867		LPDDR4-2133/2400		LPDDR4-3200		LPDDR4-4266		Units*	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data Strobe Timing											
DQS, DQS# differential output low time (DBI-Disabled)	tQSL	tCL(abs) -0.05	-	tCL(abs) -0.05	-	tCL(abs) -0.05	-	tCL(abs) -0.05	-	tCK(avg)	4,5
DQS, DQS# differential output high time (DBI-Disabled)	tQSH	tCH(abs) -0.05	-	tCH(abs) -0.05	-	tCH(abs) -0.05	-	tCH(abs) -0.05	-	tCK(avg)	4,6
DQS, DQS# differential output low time (DBI-Enabled)	tQSL_DBI	tCL(abs) -0.045	-	tCL(abs) -0.045	-	tCL(abs) -0.045	-	tCL(abs) -0.045	-	tCK(avg)	5,7
DQS, DQS# differential output high time (DBI-Enabled)	tQSH_DBI	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCK(avg)	6,7
* Unit UI = tCK(avg)min/2											

NOTE 1 DQ to DQS differential jitter where the total includes the sum of deterministic and random timing terms for a specified BER. BER specification and measurement method are TBD[1].

NOTE 2 The deterministic component of the total timing. Measurement method TBD[1].

NOTE 3 This parameter will be characterized and guaranteed by design.

NOTE 4 This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.

NOTE 5 tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge.

NOTE 6 tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge.

NOTE 7 This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.

Test Overview: The purpose of this test is to verify the width of the high level of Data Strobe signal. The limit is definable by the customers for their evaluation tests usage.

Procedure:

1 Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)

2 Take the first valid READ burst found.

3 Find all valid rising and falling DQS crossings in the said burst. (See notes on "Threshold Settings" on page 69)

4 tQSH is time started from a rising edge of the DQS and ended at the following falling edge.

5 Collect all tQSH.

6 Determine the worst result from the set of tQSH measured.

Expected/Observable Results: The worst measured tQSH shall meet the user defined limit.

tQSL Test – DQS Output Low Pulse Width

Mode Supported: DDR4 , LPDDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:
- Data Strobe Signal (supported by Data Signal)

Optional Signal(s):
- Chip Select Signal (this signal is used to separate DQS signals from different rank of memory).

Required Signals: Needed to perform this test on oscilloscope:
- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (* Optional)

References:

Specifications document	Section#	Table#
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.5	Table 92

Table 92 — Read output timings (cont'd)

Parameter	Symbol	LPDDR4-1600/1867		LPDDR4-2133/2400		LPDDR4-3200		LPDDR4-4266		Units*	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data Strobe Timing											
DQS, DQS# differential output low time (DBI-Disabled)	tQSL	tCL(abs) -0.05	-	tCL(abs) -0.05	-	tCL(abs) -0.05	-	tCL(abs) -0.05	-	tCK(avg)	4,5
DQS, DQS# differential output high time (DBI-Disabled)	tQSH	tCH(abs) -0.05	-	tCH(abs) -0.05	-	tCH(abs) -0.05	-	tCH(abs) -0.05	-	tCK(avg)	4,6
DQS, DQS# differential output low time (DBI-Enabled)	tQSL_DBI	tCL(abs) -0.045	-	tCL(abs) -0.045	-	tCL(abs) -0.045	-	tCL(abs) -0.045	-	tCK(avg)	5,7
DQS, DQS# differential output high time (DBI-Enabled)	tQSH_DBI	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCK(avg)	6,7
* Unit UI = tCK(avg)min/2											

NOTE 1 DQ to DQS differential jitter where the total includes the sum of deterministic and random timing terms for a specified BER. BER specification and measurement method are TBD[1].

NOTE 2 The deterministic component of the total timing. Measurement method TBD[1].

NOTE 3 This parameter will be characterized and guaranteed by design.

NOTE 4 This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.

NOTE 5 tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge.

NOTE 6 tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge.

NOTE 7 This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.

Test Overview: The purpose of this test is to verify the width of the low level of Data Strobe signal. The limit is definable by the customers for their evaluation tests usage.

Procedure:

1. Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)
2. Take the first valid READ burst found.
3. Find all valid rising and falling DQS crossings in the said burst. (See notes on "Threshold Settings" on page 69)
4. tQSL is time started from a falling edge of the DQS and ended at the following rising edge.
5. Collect all tQSL.
6. Determine the worst result from the set of tQSL measured.

Expected/Observable Results: The worst measured tQSL shall meet the user defined limit.

tDVAC(Strobe) Test – Time above $V_{IHdiff\ (AC)}$/ below $V_{ILdiff\ (AC)}$

Mode Supported: DDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Optional Signal(s):

- Chip Select Signal (this signal is used to separate DQS signals from different rank of memory).

Required Signals: Needed to perform this test on oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (* Optional)

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the time of strobe signal above $V_{IHdiff\ (AC)}$ and below $V_{ILdiff\ (AC)}$. The limit is definable by the customers for their evaluation tests usage.

Procedure:

1. Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)
2. Take the first valid WRITE burst found.
3. Find all valid rising and falling DQS crossings at $V_{IHdiff\ (AC)}$ and $V_{ILdiff\ (AC)}$ level in the said burst. (See notes on "Threshold Settings" on page 69)

4 tDVAC(Strobe) is time started from a DQS rising $V_{IHdiff\ (AC)}$ crosspoint and ended at the following DQS falling $V_{IHdiff\ (AC)}$ crosspoint.
5 tDVAC(Strobe) is also the time started from a DQS falling $V_{ILdiff\ (AC)}$ crosspoint and ended at the following DQS rising $V_{ILdiff\ (AC)}$ crosspoint.
6 Collect all tDVAC(Strobe).
7 Determine the worst result from the set of tDVAC(Strobe) measured.
8 Report the value of worst tDVAC(Strobe).

Expected/Observable Results: The worst measured tDVAC(Strobe) shall meet the user defined limit.

tDSS Test – DQS falling edge to CK setup time

Mode Supported: LPDDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:
- Data Strobe Signal (supported by Data Signal)
- Clock Signal

Optional Signal(s):
- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory).

Required Signals: Needed to perform this test on oscilloscope:
- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (* Optional)

References:

Specifications document	Section#	Table#	Figure#
LPDDR4 SDRAM Specification, JESD209-4, August 2014	-	-	-

Table 68 – Timing Parameters by Speed Bin

		LPDDR4-1600/ 1867		LPDDR4-2133/ 2400		LPDDR4-3200		LPDDR4-4266		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	-	-	-	-	-	-	-	-	tCK(avg)

Test Overview: The purpose of this test is to verify that the time interval from the falling edge of data strobe(DQS rising edge) output access time to clock setup time must be within the conformance limit as specified in the JEDEC specification.

Procedure:

1. Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)
2. Take the first valid WRITE burst found.
3. Find all valid rising DQS crossings in the said burst. (See notes on "Threshold Settings" on page 69)
4. For all the rising DQS crossings found, locate all nearest next rising Clock edges.
5. tDSS is the time between rising DQS crossings and the Clock rising edges found.
6. Collect all tDSS.
7. Determine the worst result from the set of tDSS measured.

Expected/Observable Results: The worst measured tDSS shall be within the specification limit.

tDSH Test – DQS falling edge hold time from CK

Mode Supported: LPDDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)
- Clock Signal

Optional Signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory).

Required Signals: Needed to perform this test on oscilloscope:

- Data Signal, DQ

- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (* Optional)

References:

Specifications document	Section#	Table#	Figure#
LPDDR4 SDRAM Specification, JESD209-4, August 2014	-	-	-

Table 68 – Timing Parameters by Speed Bin

		LPDDR4-1600/ 1867		LPDDR4-2133/ 2400		LPDDR4-3200		LPDDR4-4266		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units
DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	-	-	-	-	-	-	-	-	tCK(avg)

Test Overview: The purpose of this test is to verify that the time interval from the falling edge of data strobe output access time to hold time from clock must be within the conformance limit as specified in the JEDEC specification.

Procedure:

1. Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)
2. Take the first valid WRITE burst found.
3. Find all valid falling DQS crossings in the said burst. (See notes on "Threshold Settings" on page 69)
4. For all the falling DQS crossings found, locate all nearest prior rising Clock edges.
5. tDSH is the time between falling DQS crossings and the Clock rising edges' crossing point found.
6. Collect all tDSH.
7. Determine the worst result from the set of tDSH measured.

Expected/Observable Results: The worst measured tDSH shall be within the specification limit.

tDQSQ_DBI Test – DQS-DQ skew for DQS and associated DQ signals

Mode Supported: LPDDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)

Optional Signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory).

Required Signals: Needed to perform this test on oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (* Optional)

References:

Specifications document	Section#	Table#	Figure#
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.5	Table 92	-

Table 68 – Timing Parameters by Speed Bin

		LPDDR4-1600/ 1867		LPDDR4-2133/ 2400		LPDDR4-3200		LPDDR4-4266		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units
DQS, DQS# to DQ skew, per group, per access	tDQSQ_DB I	-	TBD	-	TBD	-	TBD	-	TBD	UI

Test Overview: The purpose of this test is to verify that the time interval from data strobe output (DQS rising and falling edge) access time to the associated data (DQ rising and falling) signal must be within the conformance limit as specified in the JEDEC specification.

Procedure:

1. Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)
2. Take the first valid READ burst found.
3. Find all valid rising and falling DQ crossings at V_{REF} in the said burst. (See notes on "Threshold Settings" on page 69)
4. For all DQ crossings found, locate the nearest DQS crossing (Rising and falling). (See notes on "Threshold Settings" on page 69)
5. Take the time different from DQ crossing to DQS crossing as the tDQSQ.
6. Determine the worst result from the set of tDQSQ measured.

Expected/Observable Results: The worst measured tDQSQ shall be within the specification limit.

tQSH_DBI Test – DQS Output High Pulse Width

Mode Supported: LPDDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Optional Signal(s):

- Chip Select Signal (this signal is used to separate DQS signals from different rank of memory).

Required Signals: Needed to perform this test on oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (* Optional)

References:

Specifications document	Section#	Table#
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.5	Table 92

Table 64 — AC Timing

Parameter	Symbol	LPDDR4-1600/1867		LPDDR4-2133/2400		LPDDR4-3200		LPDDR4-4266		Units*	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data Strobe Timing											
DQS, DQS# differential output high time (DBI-Enabled)	tQSH_DBI	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCK(avg)	6,7
* Unit UI = tCK(avg)min/2											

NOTE 1 DQ to DQS differential jitter where the total includes the sum of deterministic and random timing terms for a specified BER. BER specification and measurement method are TBD[1].

NOTE 2 The deterministic component of the total timing. Measurement method TBD[1].

NOTE 3 This parameter will be characterized and guaranteed by design.

NOTE 4 This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.

NOTE 5 tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge.

NOTE 6 tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge.

NOTE 7 This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.

Test Overview: The purpose of this test is to verify that the width of the high level of Data Strobe signal must be within the conformance limit as specified in the JEDEC specification.

Procedure:

1 Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)

2 Take the first valid READ burst found.

3 Find all valid rising and falling DQS crossings in the said burst. (See notes on "Threshold Settings" on page 69)

4 tQSH is time started from a rising edge of the DQS and ended at the following falling edge.

5 Collect all tQSH.

6 Determine the worst result from the set of tQSH measured.

Expected/Observable Results: The worst measured tQSH shall be within the specification limit.

tQSL_DBI Test – DQS Output Low Pulse Width

Mode Supported: LPDDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Optional Signal(s):

- Chip Select Signal (this signal is used to separate DQS signals from different rank of memory).

Required Signals: Needed to perform this test on oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (* Optional)

References:

Specifications document	Section#	Table#
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.5	Table 92

Table 64 — AC Timing

Parameter	Symbol	LPDDR4-1600/1867		LPDDR4-2133/2400		LPDDR4-3200		LPDDR4-4266		Units*	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data Strobe Timing											
DQS, DQS# differential output high time (DBI-Enabled)	tQSH_DBI	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCK(avg)	6,7
* Unit UI = tCK(avg)min/2											

NOTE 1 DQ to DQS differential jitter where the total includes the sum of deterministic and random timing terms for a specified BER. BER specification and measurement method are TBD[1].

NOTE 2 The deterministic component of the total timing. Measurement method TBD[1].

NOTE 3 This parameter will be characterized and guaranteed by design.

NOTE 4 This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.

NOTE 5 tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge.

NOTE 6 tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge.

NOTE 7 This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.

Test Overview: The purpose of this test is to verify that the width of the low level of Data Strobe signal must be within the conformance limit as specified in the JEDEC specification.

Procedure:

1 Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)

2 Take the first valid READ burst found.

3 Find all valid rising and falling DQS crossings in the said burst. (See notes on "Threshold Settings" on page 69)

4 tQSL is time started from a falling edge of the DQS and ended at the following rising edge.

5 Collect all tQSL.

6 Determine the worst result from the set of tQSL measured.

Expected/Observable Results: The worst measured tQSL shall be within the specification limit.

Data Timing

tDQSQ Test – DQS-DQ skew for DQS and associated DQ signals

Mode Supported: DDR4 , LPDDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)

Optional Signal(s) :

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory).

Required Signals: Needed to perform this test on oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (* Optional)

References:

Specifications document	Section#	Table#
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.5	Table 92

Table 92 — Read output timings

Parameter	Symbol	LPDDR4-1600/1867		LPDDR4-2133/2400		LPDDR4-3200		LPDDR4-4266		Units*	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data Timing											
DQS_t,DQS_c to DQ Skew total, per group, per access (DBIDisabled)	tDQSQ	-	0.18	-	0.18	-	0.18	-	0.18	UI	1
DQ output hold time total from DQS_t, DQS_c (DBI-Disabled)	tQH	min(tQSH, tQSL)	-	min(tQSH, tQSL)	-	min(tQSH, tQSL)	-	min(tQSH, tQSL)	-	UI	1
DQ output window time total, per pin (DBI-Disabled)	tQW_total	0.75	-	0.73	-	0.7	-	0.7	-	UI	1,4
DQ output window time deterministic, per pin (DBIDisabled)	tQW_dj	TBD	-	TBD	-	-	TBD	-	TBD	UI	1,4,3
DQS_t,DQS_c to DQ Skew total,per group, per access (DBI-Enabled)	tDQSQ_DBI	-	TBD	-	TBD	-	TBD	-	TBD	UI	1
DQ output hold time total from DQS_t, DQS_c (DBI-Enabled)	tQH_DBI	min(tQSH_DBI, tQSL_DBI)	-	min(tQSH_DBI, tQSL_DBI)	-	min(tQSH_DBI, tQSL_DBI)	-	min(tQSH_DBI, tQSL_DBI)	TBD	UI	1
DQ output window time total, per pin (DBI-Enabled)	tQW_total_DBI	TBD	-	TBD	-	-	TBD	-	TBD	UI	1,4

Test Overview: The purpose of this test is to verify the time interval from data strobe output(DQS rising and falling edge) access time to the associated data (DQ rising and falling) signal. The limit is definable by the customers for their evaluation tests usage.

Procedure:

1 Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)

2 Take the first valid READ burst found.

3 Find all valid rising and falling DQ crossings at V_{REF} in the said burst. (See notes on "Threshold Settings" on page 69)

4 For all DQ crossings found, locate the nearest DQS crossing (Rising and falling). (See notes on "Threshold Settings" on page 69)

5 Take the time different from DQ crossing to DQS crossing as the tDQSQ.

6 Determine the worst result from the set of tDQSQ measured.

Expected/Observable Results: The worst measured tDQSQ shall meet the user defined limit.

tQH Test – DQ/DQS output hold time from DQS

Mode Supported: DDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)

Optional Signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory).

Required Signals: Needed to perform this test on oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (* Optional)

References:

Specifications document	Section#	Table#
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.5	Table 92

Table 92 — Read output timings

Parameter	Symbol	LPDDR4-1600/1867		LPDDR4-2133/2400		LPDDR4-3200		LPDDR4-4266		Units*	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data Timing											
DQS_t,DQS_c to DQ Skew total, per group, per access (DBIDisabled)	tDQSQ	-	0.18	-	0.18	-	0.18	-	0.18	UI	1
DQ output hold time total from DQS_t, DQS_c (DBI-Disabled)	tQH	min(tQSH, tQSL)	-	min(tQSH, tQSL)	-	min(tQSH, tQSL)	-	min(tQSH, tQSL)	-	UI	1
DQ output window time total, per pin (DBI-Disabled)	tQW_total	0.75	-	0.73	-	0.7	-	0.7	-	UI	1,4
DQ output window time deterministic, per pin (DBIDisabled)	tQW_dj	TBD	-	TBD	-	-	TBD	-	TBD	UI	1,4,3
DQS_t,DQS_c to DQ Skew total,per group, per access (DBI-Enabled)	tDQSQ_DBI	-	TBD	-	TBD	-	TBD	-	TBD	UI	1
DQ output hold time total from DQS_t, DQS_c (DBI-Enabled)	tQH_DBI	min(tQSH_DBI, tQSL_DBI)	-	min(tQSH_DBI, tQSL_DBI)	-	min(tQSH_DBI, tQSL_DBI)	-	min(tQSH_DBI, tQSL_DBI)	TBD	UI	1
DQ output window time total, per pin (DBI-Enabled)	tQW_total_DBI	TBD	-	TBD	-	-	TBD	-	TBD	UI	1,4

Test Overview: The purpose of this test is to verify the time interval from data output hold time (DQ rising and falling edge) from DQS(rising/falling edge). The limit is definable by the customers for their evaluation tests usage.

Procedure:

1. Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)
2. Take the first valid READ burst found.
3. Find all valid rising and falling DQ crossings at V_{REF} in the said burst. (See notes on "Threshold Settings" on page 69)
4. For all DQ crossings found, locate the nearest DQS rising crossing. (See notes on "Threshold Settings" on page 69).
5. Using the found DQS rising crossing, locate the DQS rising crossing prior.
6. Take the time different from DQ crossing to DQS crossing found as the tQH.
7. Determine the worst result from the set of tQH measured.

Expected/Observable Results: The worst measured tQH shall meet the user defined limit.

tLZ(DQ) Test – DQ low-impedance time from CK,/CK

Mode Supported: DDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)
- Clock Signal (CK as Reference Signal)

Optional Signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Required Signals: Needed to perform this test on oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (* Optional)

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the time when DQ start driving (*from High-impedance state to High/Low state) to the clock signal crossing. The limit is definable by the customers for their evaluation tests usage.

Procedure:

1. Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)
2. Take the first valid READ burst found.

3 Find tLZBeginPoint of the said burst. (See notes on "Finding tLZBeginPoint(DQ)" on page 76)
4 Find the nearest Clock rising edge.
5 tLZ(DQ) is the time interval of the found clock rising edge's crossing point to the tLZBeginPoint found.
6 Report tLZ(DQ).

Expected/Observable Results: The measured tLZ(DQ) shall meet the user defined limit.

tHZ(DQ) Test – DQ out high-impedance time from CK,/CL

Mode Supported: DDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)
- Clock Signal (CK as Reference Signal)

Optional Signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Required Signals: Needed to perform this test on oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (* Optional)

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the time when DQ no longer driving(*from High state OR Low state to the High-impedance state) to the clock signal crossing. The limit is definable by the customers for their evaluation tests usage.

Procedure:

1 Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)
2 Take the first valid READ burst found.
3 Find tHZEndPoint of the said burst. (See notes on "Find tHZEndPoint(DQ)" on page 77)
4 Find the nearest Clock rising crossing.

5 tHZ(DQ) is the time interval of the found Clock rising edge's crossing point to the tHZEndPoint found.
6 Report tHZ(DQ).

Expected/Observable Results: The measured tHZ(DQ) shall meet the user defined limit.

tDIPW Test – DQ and DM input pulse width

Mode Supported: DDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal) OR
- Data Mask Signal

Optional Signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory).

Required Signals: Needed to perform this test on oscilloscope:

- Data Signal, DQ or Data Mask Signal, DM
- Data Strobe Signal, DQS
- Chip Select Signal, CS (* Optional)

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the width of the high or low level of Data signal. The limit is definable by the customers for their evaluation tests usage.

Procedure:

1 Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)
2 Take the first valid WRITE burst found.
3 Find all valid rising and falling DQ crossings at V_{REF} in the said burst. (See notes on "Threshold Settings" on page 69)
4 tDIPW is time started from a rising/falling edge of the DQ and ended at the following falling/rising (following edge should not same direction) edge.
5 Collect all tDIPW.
6 Determine the worst result from the set of tDIPW measured.

Expected/Observable Results: The worst measured tDIPW shall meet the user defined limit.

tQH_DBI Test – DQ/DQS output hold time from DQS

Mode Supported: LPDDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:
- Data Signal (supported by Data Strobe Signal)

Optional Signal(s):
- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory).

Required Signals: Needed to perform this test on oscilloscope:
- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (* Optional)

References:

Specifications document	Section#	Table#	Figure#
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.5	Table 92	-

Table 68 – Timing Parameters by Speed Bin

		LPDDR4-1600/ 1867		LPDDR4-2133/ 2400		LPDDR4-3200		LPDDR4-4266		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units
DQ output hold time from DQS, DQS#	tQH_DBI	Min(tQSH_DBI, tQSL_DBI)	-	Min(tQSH_DBI, tQSL_DBI)	-	Min(tQSH_DBI, tQSL_DBI)	-	Min(tQSH_DBI, tQSL_DBI)	-	tCK(avg)

Test Overview: The purpose of this test is to verify that the time interval from data output hold time (DQ rising and falling edge) from DQS(rising/falling edge) must be within the conformance limit as specified in the JEDEC specification.

Procedure:

1. Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)
2. Take the first valid READ burst found.

3 Find all valid rising and falling DQ crossings at V_{REF} in the said burst. (See notes on "Threshold Settings" on page 69)
4 For all DQ crossings found, locate the nearest DQS rising crossing. (See notes on "Threshold Settings" on page 69).
5 Using the found DQS rising crossing, locate the DQS rising crossing prior.
6 Take the time different from DQ crossing to DQS crossing found as the tQH.
7 Determine the worst result from the set of tQH measured.

Expected/Observable Results: The worst measured tQH shall be within the specification limit.

tDIPW Test – DQ and DM input pulse width

Mode Supported: LPDDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal) OR
- Data Mask Signal

Optional Signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory).

Required Signals: Needed to perform this test on oscilloscope:

- Data Signal, DQ or Data Mask Signal, DM
- Data Strobe Signal, DQS
- Chip Select Signal, CS (* Optional)

References:

Specifications document	Section#	Table#
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.6	Table 94

Table 94 — DRAM DQs In Receive Mode

Symbol	Parameter	1600/1867[A]		2133/2400		3200		4266		Unit	NOTE
		min	max	min	max	min	max	min	max		
VdIVW_total	Rx Mask voltage - p-p total	-	140	-	140	-	140	-	120	mV	1,2,3,5
TdIVW_total	Rx timing window total (At VdIVW voltage levels)	-	0.22	-	0.22	-	0.25	-	0.25	UI*	1,2,4,5
TdIVW_1bit	Rx timing window 1 bit toggle (At VdIVW voltage levels)	-	TBD	-	TBD	-	TBD	-	TBD	UI*	1,2,4, 5,14
VIHL_AC	DQ AC input pulse amplitude pk-pk	180	-	180	-	180	-	170	-	mV	7,15
TdIPW DQ	Input pulse width (At Vcent_DQ)	0.45		0.45		0.45		0.45		UI*	8
tDQS2DQ	DQ to DQS offset	200	800	200	800	200	800	200	800	ps	9
tDQDQ	DQ to DQ offset	-	30	-	30	-	30	-	30	ps	10
tDQS2DQ_temp	DQ to DQS offset temperature variation	-	0.6	-	0.6	-	0.6	-	0.6	ps/°C	11
tDQS2DQ_volt	DQ to DQS offset voltage variation	-	33	-	33	-	33	-	33	ps/50mV	12
SRIN_dIVW	Input Slew Rate over VdIVW_total	1	7	1	7	1	7	1	7	V/ns	13

* UI = tCK(avg)min/2

A The following Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. For example the TcIVW(ps) = 450ps at or below 1333 operating frequencies.

Test Overview: The purpose of this test is to verify the width of the high or low level of Data signal. The limit is definable by the customers for their evaluation tests usage.

Procedure:

1. Acquire and split read and write burst of the acquired signal. (See notes on "DDR Read/Write Separation" on page 62)
2. Take the first valid WRITE burst found.
3. Find all valid rising and falling DQ crossings at V_{REF} in the said burst. (See notes on "Threshold Settings" on page 69)
4. tDIPW is time started from a rising/falling edge of the DQ and ended at the following falling/rising (following edge should not same direction) edge.
5. Collect all tDIPW.
6. Determine the worst result from the set of tDIPW measured.

Expected/Observable Results: The worst measured tDIPW shall meet the user defined limit.

Command Address Timing (CAT)

tIS(base) Test – Address and control input setup time

Mode Supported: DDR4

Signal cycle of interest: WRITE

Require Read/Write separation: No

Signal(s) of Interest:

- Address Signal OR Control Signal
- Clock Signal

Required Signals: Needed to perform this test on oscilloscope:

- Address Signal or Control Signal
- Clock Signal

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the time interval from address or control (Add/Ctrl rising/falling edge) setup time to the associated clock crossing edge. You may define the limits for evaluation tests usage.

Procedure:

1. Pre-condition the oscilloscope.
2. Trigger on either rising or falling edge of the address/control signal under test.
3. Find all crossings on rising edge of the signal under test that cross Vih(ac).
4. Find all crossings on falling edge of the signal under test that cross Vil(ac).
5. For all the crossings found, locate the nearest Clock crossings that cross 0V.
6. Note the difference in time of the signal under test's crossings to the corresponding clock's crossing and record this time difference as tIS.
7. Collate all the measured values of tIS.
8. Report the “worst” measured value of tIS as the test result.

Expected/Observable Results: The measured time interval between address/control (Add/Ctrl) setup time to respective clock crossing point shall meet the user defined limit.

tIH(base) Test – Address and control input hold time

Mode Supported: DDR4

Signal cycle of interest: WRITE

Require Read/Write separation: No

Signal(s) of Interest:

- Address Signal OR Control Signal
- Clock Signal

Required Signals: Needed to perform this test on oscilloscope:

- Address Signal or Control Signal
- Clock Signal

References: There is no limit found for this test.

Test Overview: The purpose of this test is to verify the time interval from address or control (Add/Ctrl rising/falling edge) hold time to the associated clock crossing edge. You may define the limits for evaluation tests usage.

Procedure:

1. Pre-condition the oscilloscope.
2. Trigger on either rising or falling edge of the address/control signal under test.
3. Find all crossings on rising edge of the signal under test that cross Vil(dc).
4. Find all crossings on falling edge of the signal under test that cross Vih(dc).
5. For all the crossings found, locate the nearest Clock crossings that cross 0V.
6. Take the time different of the signal under test's crossings to the corresponding clock crossing as tIH.
7. Collect all measured tIH.
8. Report the worst tIH measured as test result.
9. Compare the test result to the compliance test limit.

Expected/Observable Results: The measured time interval between address/control(Add/Ctrl) hold time to respective clock crossing point shall meet the user defined limit.

tCKE Test – CKE Minimum Pulse Width

Mode Supported: DDR4

Signal cycle of interest: WRITE

Require Read/Write separation: No

Signal(s) of Interest:

- CKE Signal

Required Signals: Needed to perform this test on oscilloscope:

- CKE Signal

- Clock Signal

References:

Specifications document	Section#	Table#
DDR4 SDRAM Specification, JESD79-4, September 2012	12	Table 101 and 102

Table 101 — Timing Parameters by Speed Bin for DDR4-1600 to DDR4-2133

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Data Strobe Timing									
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-		31,32

Table 102 — Timing Parameters by Speed Bin for DDR4-2400 to DDR4-3200

Speed		DDR4-2400		DDR4-2666		DDR4-3200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Power Down Timing									
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	TBD	-	TBD	-		31,32

Test Overview: The purpose of this test is to verify that the pulse width of CKE signal is within the conformance limit as specified in the JEDEC specification.

Procedure:

1. Pre-condition the oscilloscope.
2. Trigger on either rising or falling edge of the command/address/control signal under test.
3. Find all crossings on the rising/falling edge of the CKE signal that cross V_{REF}.
4. Find all crossings on the rising edge of the Clock signal that cross V_{REF}.
5. Find the rising edge of Clock (ClkEdge1), which is nearest to the right side of the first rising/falling edge of the CKE signal.
6. Find the rising edge of Clock (ClkEdge2), which is nearest to the right side of the second rising/falling edge of the CKE signal.
7. Calculate tCKE = ClkEdge2- ClkEdge1.
8. Repeat steps 5 to 7 for all CKE crossings found in steps 2 and 3.
9. Determine the “worst” value from the set of measured tCKE values for the final test result.
10. Report the worst value of tCKE for the final test result.

Expected/Observable Results: The “worst” value of the measured CKE shall be within the specification limits.

tCIVW Test for Write Cycle

Mode Supported: LPDDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signals (supported by Data Strobe Signals)

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = CA Signals.

References:

Specifications document	Section#	Table#
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.4	Table 91

Table 91 — DRAM CMD/ADR, CS

Symbol	Parameter	DQ-1333[A]		DQ-1600/1867		DQ-3200		DQ-4266		Unit	NOTE
		min	max	min	max	min	max	min	max		
VcIVW	Rx Mask voltage - p-p	-	175	-	175	-	155	-	145	mV	1,2,4
TcIVW	Rx timing window	-	0.3	-	0.3	-	0.3	-	0.3	UI*	1,2,3,4
VIHL_AC	CA AC input pulse amplitude pk-pk	210	-	210	-	190	-	180	-	mV	5,8
TcIPW	CA input pulse width	0.55		0.55		0.6		0.6		UI*	6
SRIN_cIVW	Input Slew Rate over VcIVW	1	7	1	7	1	7	1	7	V/ns	7

* UI = tck(avg)min

[A] The following Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. For example the TcIVW(ps) = 450ps at or below 1333 operating frequencies.

NOTE 1 CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.

NOTE 2 Rx mask voltage VcIVW total(max) must be centered around Vcent_CA(pin mid).

NOTE 3 Rx differential CA to CK jitter total timing window at the VcIVW voltage levels.

NOTE 4 Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal V_{REF} CA range irrespective of the input signal common mode.

NOTE 5 CA only input pulse signal amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_CA(pin mid) such that VIHL_AC/2 min must be met both above and below Vcent_CA.

NOTE 6 CA only minimum input pulse width defined at the Vcent_CA(pin mid).

NOTE 7 Input slew rate over VcIVW Mask centered at Vcent_CA(pin mid).

NOTE 8 VIHL_AC does not have to be met when no transitions are occurring.

Test Overview: The purpose of this test is to automate all the setup procedures required to generate an eye diagram for the LPDDR4 data WRITE cycle.

Using the mask test, you may perform evaluations and debugging on the generated eye diagram.

Procedure:

1. Calculate the value of the initial time scale based on the selected LPDDR4 speed grade options.
2. Calculate the number of sampling points according to the time scale value.
3. Check for valid DQS input test signals by verifying their frequency and amplitude values.
4. On the Oscilloscope:
   - **a** Use the UDF methodology to separate the Write bursts and to return the filtered DQ signals as recovered clock signals, which is used for eye folding later.
   - **b** Set up measurement threshold values for the DQx channel, CAx channel and the DQSx channel input.
   - **c** Set up fixed vertical scale values for DQx channel, CAx channel and DQSx channel input.
   - **d** Identify the Vcent of CA signal.
   - **e** Identify the X1 value for re-adjustment of the selected test mask.
   - **f** Set up Mask Test settings (Load default Test Mask on screen).
   - **g** Set up Clock Recovery settings on SDA.

     : Explicit clock, Source = DQS, Rise/Fall Edge
   - **h** Set the Real Time Eye on SDA to ON.
5. Perform Mask Testing:
   - **a** Set the termination condition of the Mask Test to ‘Waveforms’ and define the number of waveforms to be acquired.
   - **b** Start the Mask Test.
6. Loop until number of required waveforms is acquired.
7. Acquire the value of Vcent. Use the **Vcent Evaluation Mode** configuration to derive upon a value for Vcent such that:
   - **a** Setting the **Vcent Evaluation Mode** configuration to **User defined Vcent** configures the value of Vcent to that defined by the user.
   - **b** Setting the **Vcent Evaluation Mode** configuration to **Widest eye opening level** configures the value of Vcent based on the level of widest eye opening on the eye diagram.
8. In the **Widest eye opening level** configuration:
   - **a** Measure Vmin and Vmax.
   - **b** Based on the values of Vmin and Vmax, the search of the level for values of Vcent ranges from 40% to 60% of the level between Vmax and Vmin. Mathematically, the levels of Vcent are calculated as:

     VcentSearchStart = Vmin + 0.6 * (Vmax - Vmin)

VcentSearchEnd = Vmin + 0.4 * (Vmax - Vmin)

c Find the eye opening at VcentSearchStart and store the level and eye opening width. Repeat this step for eye openings at VcentSearchStart+5mV, VcentSearchStart+10mV, VcentSearchStart+15mV and so on till VcentSearchEnd.

d Find the level of the widest eye opening from the stored eye opening width measurements. Record the derived value as Vcent.

9 To adjust the default rectangular Test Mask, perform the following modifications:

a Upper Mask Level = Vcent + (0.5 x Compliance_vCivw_Value).

For Compliance_vCivw_Value of 136mV, Upper Mask Level = Vcent + 68mV.

b Lower Mask Level = Vcent - (0.5 x Compliance_vCivw_Value).

For Compliance_vCivw_Value of 136mV, Lower Mask Level = Vcent - 68mV.

c Right Mask Position = TimePosition + (0.5 x Compliance_tCivw_Value).

or, Right Mask Position = TimePosition + (0.5 x UI).

d Left Mask Position = TimePosition - (0.5 x Compliance_tCivw_Value).

or, Left Mask Position = TimePosition - (0.5 x UI).

10 Measure tCIVW margin on the upper right corner of the mask:

a Set up Histogram window in the following manner:

- Left window: 0s (Center position of the Eye/Mask).
- Right window: Right side of the grid.
- Upper window: Top Level of Mask.
- Lower window: Top Level of Mask.

b Measure horizontal Histogram Min.

c Calculate:

tCIVW margin upper right = 100% x (Histogram_Min - 0.5 x Compliance_tCivw_Value) / (0.5 x Compliance_tCivw_Value)

11 Measure tCIVW margin on the upper left corner of the mask:

a Set up Histogram window in the following manner:

- Left window: Left side of the grid.
- Right window: 0s (Center position of the Eye/Mask).
- Upper window: Top Level of Mask.
- Lower window: Top Level of Mask.

b Measure horizontal Histogram Max.

c Calculate:

tCIVW margin upper left = 100% x [(- 0.5 x Compliance_tCivw_Value) - Histogram_Max] / (0.5 x Compliance_tCivw_Value)

12 Measure tCIVW margin on the lower right corner of the mask:

a Set up Histogram window in the following manner:

- Left window: 0s (Center position of the Eye/Mask).
- Right window: Right side of the grid.
- Upper window: Bottom Level of Mask.
- Lower window: Bottom Level of Mask.

b Measure horizontal Histogram Min.

c Calculate:

tCIVW margin lower right = 100% x (Histogram_Min - 0.5 x Compliance_tCivw_Value) / (0.5 x Compliance_tCivw_Value)

13 Measure tCIVW margin on the lower left corner of the mask:

a Set up Histogram window in the following manner:

- Left window: Left side of the grid.
- Right window: 0s (Center position of the Eye/Mask).
- Upper window: Bottom Level of Mask.
- Lower window: Bottom Level of Mask.

b Measure horizontal Histogram Max.

c Calculate:

tCIVW margin lower left = 100% x [(- 0.5 x Compliance_tCivw_Value) - Histogram_Max] / (0.5 x Compliance_tCivw_Value)

14 For the worst result, note the minimal value between tCIVW margin upper left, tCIVW margin upper right, tCIVW margin lower left and tCIVW margin lower right.

15 Report the worst result as the test result.

Expected/Observable Results: Generation of an eye diagram for the LPDDR4 data WRITE cycle and loading of a default test mask pattern.

The test will show a FAIL status if the total failed waveforms is greater than 0 and the tCIVW min, VcentCA , tCIVW top, and tCIVW bottom are reported.

vCIVW Margin Test for Write Cycle

Mode Supported: LPDDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signals (supported by Data Strobe Signals)

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = CA Signals.

References:

Specifications document	Section#	Table#
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.4	Table 91

Table 91 — DRAM CMD/ADR, CS

Symbol	Parameter	DQ-1333[A]		DQ-1600/1867		DQ-3200		DQ-4266		Unit	NOTE
		min	max	min	max	min	max	min	max		
VcIVW	Rx Mask voltage - p-p	-	175	-	175	-	155	-	145	mV	1,2,4
TcIVW	Rx timing window	-	0.3	-	0.3	-	0.3	-	0.3	UI*	1,2,3,4
VIHL_AC	CA AC input pulse amplitude pk-pk	210	-	210	-	190	-	180	-	mV	5,8
TcIPW	CA input pulse width	0.55		0.55		0.6		0.6		UI*	6
SRIN_cIVW	Input Slew Rate over VcIVW	1	7	1	7	1	7	1	7	V/ns	7
* UI = tck(avg)min											
A The following Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. For example the TcIVW(ps) = 450ps at or below 1333 operating frequencies.											

NOTE 1 CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.

NOTE 2 Rx mask voltage VcIVW total(max) must be centered around Vcent_CA(pin mid).

NOTE 3 Rx differential CA to CK jitter total timing window at the VcIVW voltage levels.

NOTE 4 Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal V_{REF} CA range irrespective of the input signal common mode.

NOTE 5 CA only input pulse signal amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_CA(pin mid) such that VIHL_AC/2 min must be met both above and below Vcent_CA.

NOTE 6 CA only minimum input pulse width defined at the Vcent_CA(pin mid).

NOTE 7 Input slew rate over VcIVW Mask centered at Vcent_CA(pin mid).

NOTE 8 VIHL_AC does not have to be met when no transitions are occurring.

Test Overview: The purpose of this test is to automate all the setup procedures required to generate an eye diagram for the LPDDR4 data WRITE cycle.

Using the mask test, you may perform evaluations and debugging on the generated eye diagram.

Procedure:

1 Calculate the value of the initial time scale based on the selected LPDDR4 speed grade options.

2 Calculate the number of sampling points according to the time scale value.

3 Check for valid DQS input test signals by verifying their frequency and amplitude values.

4 On the Oscilloscope:

   a Use the UDF methodology to separate the Write bursts and to return the filtered DQ signals as recovered clock signals, which is used for eye folding later.

   b Set up measurement threshold values for the DQx channel, CAx channel and the DQSx channel input.

   c Set up fixed vertical scale values for DQx channel, CAx channel and DQSx channel input.

   d Set the Color Grade Display Option to ON.

   e Identify the Vcent of CA signal.

   f Identify the X1 value for re-adjustment of the selected test mask.

   g Set up Mask Test settings (Load default Test Mask on screen).

   h Set up Clock Recovery settings on SDA.

   : Explicit clock, Source = DQS, Rise/Fall Edge

   i Set the Real Time Eye on SDA to ON.

5 Perform Mask Testing:

   a Set the termination condition of the Mask Test to ‘Waveforms’ and define the number of waveforms to be acquired.

   b Start the Mask Test.

6 Set up a Histogram to find vCIVW top, vCIVW bottom and worst vCIVW margin.

7 Loop until number of required waveforms is acquired.

8 Acquire the value of Vcent. Use the **Vcent Evaluation Mode** configuration to derive upon a value for Vcent such that:

   a Setting the **Vcent Evaluation Mode** configuration to **User defined Vcent** configures the value of Vcent to that defined by the user.

   b Setting the **Vcent Evaluation Mode** configuration to **Widest eye opening level** configures the value of Vcent based on the level of widest eye opening on the eye diagram.

9 In the **Widest eye opening level** configuration:

   a Measure Vmin and Vmax.

   b Based on the values of Vmin and Vmax, the search of the level for values of Vcent ranges from 40% to 60% of the level between Vmax and Vmin. Mathematically, the levels of Vcent are calculated as:

VcentSearchStart = Vmin + 0.6 * (Vmax - Vmin)

VcentSearchEnd = Vmin + 0.4 * (Vmax - Vmin)

c Find the eye opening at VcentSearchStart and store the level and eye opening width. Repeat this step for eye openings at VcentSearchStart+5mV, VcentSearchStart+10mV, VcentSearchStart+15mV and so on till VcentSearchEnd.

d Find the level of the widest eye opening from the stored eye opening width measurements. Record the derived value as Vcent.

10 To adjust the default rectangular Test Mask, perform the following modifications:

a Upper Mask Level = Vcent + (0.5 x Compliance_vCivw_Value).

For Compliance_vCivw_Value of 136mV, Upper Mask Level = Vcent + 68mV.

b Lower Mask Level = Vcent - (0.5 x Compliance_vCivw_Value).

For Compliance_vCivw_Value of 136mV, Lower Mask Level = Vcent - 68mV.

c Right Mask Position = TimePosition + (0.5 x Compliance_tCivw_Value).

or, Right Mask Position = TimePosition + (0.5 x UI).

d Left Mask Position = TimePosition - (0.5 x Compliance_tCivw_Value).

or, Left Mask Position = TimePosition - (0.5 x UI).

11 Measure vCIVW margin on the upper side of the mask:

a Set up Histogram window in the following manner:

- Left window: -0.5 x Compliance_tCivw_Value.
- Right window: 0.5 x Compliance_tCivw_Value.
- Upper window: Vmax of the CA signal (measured earlier).
- Lower window: Vcent (measured earlier).

b Measure Histogram Min.

c Calculate:

vCIVW margin upper = 100% x (Histogram_Min - Upper Level of Mask) / (0.5 x Compliance_vCivw_Value)

12 Measure vCIVW margin on the lower side of the mask:

a Set up Histogram window in the following manner:

- Left window: -0.5 x Compliance_tCivw_Value.
- Right window: 0.5 x Compliance_tCivw_Value.
- Upper window: Vcent (measured earlier).

- Lower window: Vmin of the CA signal (measured earlier).

b Measure Histogram Max.

c Calculate:

vCIVW margin lower = 100% x (Bottom Level of Mask - Histogram_Max) / (0.5 x Compliance_vCivw_Value)

13 For the worst result, note the minimal value between vCIVW margin upper and vCIVW margin lower.

14 Report the worst result as the test result.

Expected/Observable Results: Generation of an eye diagram for the LPDDR4 data WRITE cycle and loading of a default test mask pattern.

The test will show a FAIL status if the total failed waveforms is greater than zero and the worst vCIVW margin value, vCIVW top and vCIVW bottom are reported.

CA VIHL(ac) Test for Write Cycle

Mode Supported: LPDDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signals (supported by Command Address Signals)

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = CA Signals.

References:

Specifications document	Section#	Table#
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.4	Table 91

Table 91 — DRAM CMD/ADR, CS

Symbol	Parameter	DQ-1333[A]		DQ-1600/1867		DQ-3200		DQ-4266		Unit	NOTE
		min	max	min	max	min	max	min	max		
VcIVW	Rx Mask voltage - p-p	-	175	-	175	-	155	-	145	mV	1,2,4
TcIVW	Rx timing window	-	0.3	-	0.3	-	0.3	-	0.3	UI*	1,2,3,4
VIHL_AC	CA AC input pulse amplitude pk-pk	210	-	210	-	190	-	180	-	mV	5,8
TcIPW	CA input pulse width	0.55		0.55		0.6		0.6		UI*	6
SRIN_cIVW	Input Slew Rate over VcIVW	1	7	1	7	1	7	1	7	V/ns	7

* UI = tck(avg)min

[A] The following Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. For example the TcIVW(ps) = 450ps at or below 1333 operating frequencies.

NOTE 1 CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.

NOTE 2 Rx mask voltage VcIVW total(max) must be centered around Vcent_CA(pin mid).

NOTE 3 Rx differential CA to CK jitter total timing window at the VcIVW voltage levels.

NOTE 4 Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal V_{REF} CA range irrespective of the input signal common mode.

NOTE 5 CA only input pulse signal amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_CA(pin mid) such that VIHL_AC/2 min must be met both above and below Vcent_CA.

NOTE 6 CA only minimum input pulse width defined at the Vcent_CA(pin mid).

NOTE 7 Input slew rate over VcIVW Mask centered at Vcent_CA(pin mid).

NOTE 8 VIHL_AC does not have to be met when no transitions are occurring.

Test Overview: The purpose of this test is to automate all the setup procedures required to generate an eye diagram for the LPDDR4 data CA cycle.

Using the mask test, you may perform evaluations and debugging on the generated eye diagram.

Procedure:

1. Calculate the value of the initial time scale based on the selected LPDDR4 speed grade options.
2. Calculate the number of sampling points according to the time scale value.
3. Check for valid CA input test signals by verifying their frequency and amplitude values.

4 On the Oscilloscope:
   a Use the UDF methodology to separate the Write bursts and to return the filtered DQ signals as recovered clock signals, which is used for eye folding later.
   b Set up measurement threshold values for the DQx channel, CAx channel and the DQSx channel input.
   c Set up fixed vertical scale values for DQx channel, CAx channel and DQSx channel input.
   d Set the Color Grade Display option to ON.
   e Identify the Vcent of CA signal.
   f Identify the X1 value for re-adjustment of the selected test mask.
   g Set up Mask Test settings (Load default Test Mask on screen).
   h Set up Clock Recovery settings on SDA.

      : Explicit clock, Source = DQ, Rise/Fall Edge
   i Set the Real Time Eye on SDA to ON.
5 Perform Mask Testing:
   a Set the termination condition of the Mask Test to ‘Waveforms’ and define the number of waveforms to be acquired.
   b Start the Mask Test.
6 Loop until number of required waveforms is acquired.
7 Acquire the value of Vcent. Use the **Vcent Evaluation Mode** configuration to derive upon a value for Vcent such that:
   a Setting the **Vcent Evaluation Mode** configuration to **User defined Vcent** configures the value of Vcent to that defined by the user.
   b Setting the **Vcent Evaluation Mode** configuration to **Widest eye opening level** configures the value of Vcent based on the level of widest eye opening on the eye diagram.
8 In the **Widest eye opening level** configuration:
   a Measure Vmin and Vmax.
   b Based on the values of Vmin and Vmax, the search of the level for values of Vcent ranges from 40% to 60% of the level between Vmax and Vmin. Mathematically, the levels of Vcent are calculated as:

$$VcentSearchStart = Vmin + 0.6 * (Vmax - Vmin)$$

$$VcentSearchEnd = Vmin + 0.4 * (Vmax - Vmin)$$

   c Find the eye opening at VcentSearchStart and store the level and eye opening width. Repeat this step for eye openings at VcentSearchStart+5mV, VcentSearchStart+10mV, VcentSearchStart+15mV and so on till VcentSearchEnd.

   d Find the level of the widest eye opening from the stored eye opening width measurements. Record the derived value as Vcent.

9 Set up a Histogram to find the CAVIHL top and CAVIHL bottom.

10 To find CAVIHL top and CAVIHL bottom, configure:

   a TimePos = Current Time Position

   b VIHLScanStart = TimePos - 0.5UI

   c VIHLScanEnd = TimePos + 0.5UI

   d VIHLStepScan = 10e-12

   e NoOfStepVIHL = 0

   f Calculate CurrentTime, where

      CurrentTime = VIHLScanStart + NoOfStepVIHL x VIHLStepScan.

   g Set up the top Histogram window in the following manner:

   - Left window: CurrentTime + (VIHLStepScan / 2).
   - Right window: CurrentTime - (VIHLStepScan / 2).
   - Upper window: Vmax of the CA signal (measured earlier).
   - Lower window: Vcent (measured earlier).

   h Measure Histogram Min.

   i Set up the bottom Histogram window in the following manner:

   - Left window: CurrentTime + (VIHLStepScan / 2).
   - Right window: CurrentTime - (VIHLStepScan / 2).
   - Upper window: Vcent (measured earlier).
   - Lower window: Vmin of the CA signal (measured earlier).

   j Measure Histogram Max.

   k Repeat the procedure of setting up of Histogram window by incrementing the value of NoOfStepVIHL by one for each trial until the value of CurrentTime exceeds that of VIHLScanEnd.

   l Once the value of CurrentTime exceeds that of VIHLScanEnd, stop the procedure of setting up of the Histogram window. Record the maximum value of the top Histogram window as CAVIHL top and the minimum value of the bottom Histogram window as CAVIHL bottom.

11 Report the values for CAVIHL top and CAVIHL bottom as the final test result.

Expected/Observable Results: Generation of an eye diagram for the LPDDR4 data CA cycle and loading of a default test mask pattern.

The test will show a FAIL status if the total failed waveforms is greater than zero and the CAVIHL top and CAVIHL bottom value will be reported.

tCIPW Test for Write Cycle

Mode Supported: LPDDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signals (supported by Commands Address Signals)

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = CA Signals.

References:

Specifications document	Section#	Table#
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.4	Table 91

Table 91 — DRAM CMD/ADR, CS

Symbol	Parameter	DQ-1333[A]		DQ-1600/1867		DQ-3200		DQ-4266		Unit	NOTE
		min	max	min	max	min	max	min	max		
VcIVW	Rx Mask voltage - p-p	-	175	-	175	-	155	-	145	mV	1,2,4
TcIVW	Rx timing window	-	0.3	-	0.3	-	0.3	-	0.3	UI*	1,2,3,4
VIHL_AC	CA AC input pulse amplitude pk-pk	210	-	210	-	190	-	180	-	mV	5,8
TcIPW	CA input pulse width	0.55		0.55		0.6		0.6		UI*	6
SRIN_cIVW	Input Slew Rate over VcIVW	1	7	1	7	1	7	1	7	V/ns	7
* UI = tck(avg)min											
A The following Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. For example the TcIVW(ps) = 450ps at or below 1333 operating frequencies.											

NOTE 1 CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.

NOTE 2 Rx mask voltage VcIVW total(max) must be centered around Vcent_CA(pin mid).

NOTE 3 Rx differential CA to CK jitter total timing window at the VcIVW voltage levels.

NOTE 4 Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal V_{REF} CA range irrespective of the input signal common mode.

NOTE 5 CA only input pulse signal amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_CA(pin mid) such that VIHL_AC/2 min must be met both above and below Vcent_CA.

NOTE 6 CA only minimum input pulse width defined at the Vcent_CA(pin mid).

NOTE 7 Input slew rate over VcIVW Mask centered at Vcent_CA(pin mid).

NOTE 8 VIHL_AC does not have to be met when no transitions are occurring.

Test Overview: The purpose of this test is to automate all the setup procedures required to generate an eye diagram for the LPDDR4 data Command Address cycle.

Using the mask test, you may perform evaluations and debugging on the generated eye diagram.

Procedure:

1 Calculate the value of the initial time scale based on the selected LPDDR4 speed grade options.

2 Calculate the number of sampling points according to the time scale value.

3 Check for valid CA input test signals by verifying their frequency and amplitude values.

4 On the Oscilloscope:

  a Set up measurement threshold values for the CAx channel.

  b Set up fixed vertical scale values for CAx channel input.

  c Set the Color Grade Display option to ON.

  d Identify the X1 value for re-adjustment of the selected test mask.

  e Set up Mask Test settings (Load default Test Mask on screen).

  f Set up Clock Recovery settings on SDA.

  : Explicit clock, Source = DQ, Rise/Fall Edge

  g Set the Real Time Eye on SDA to ON.

5 Perform Mask Testing:

  a Set the termination condition of the Mask Test to ‘Waveforms’ and define the number of waveforms to be acquired.

  b Start the Mask Test.

6 Loop until number of required waveforms is acquired.

7 Acquire the value of Vcent. Use the **Vcent Evaluation Mode** configuration to derive upon a value for Vcent such that:

  a Setting the **Vcent Evaluation Mode** configuration to **User defined Vcent** configures the value of Vcent to that defined by the user.

  b Setting the **Vcent Evaluation Mode** configuration to **Widest eye opening level** configures the value of Vcent based on the level of widest eye opening on the eye diagram.

8 In the **Widest eye opening level** configuration:

  a Measure Vmin and Vmax.

  b Based on the values of Vmin and Vmax, the search of the level for values of Vcent ranges from 40% to 60% of the level between Vmax and Vmin. Mathematically, the levels of Vcent are calculated as:

$$\text{VcentSearchStart} = \text{Vmin} + 0.6 * (\text{Vmax} - \text{Vmin})$$

$$\text{VcentSearchEnd} = \text{Vmin} + 0.4 * (\text{Vmax} - \text{Vmin})$$

  c Find the eye opening at VcentSearchStart and store the level and eye opening width. Repeat this step for eye openings at VcentSearchStart+5mV, VcentSearchStart+10mV, VcentSearchStart+15mV and so on till VcentSearchEnd.

- **d** Find the level of the widest eye opening from the stored eye opening width measurements. Record the derived value as Vcent.

9 Measure the positive pulse width and the negative pulse width of the CA signal. Find the smaller or the worst value of the CA signal pulse width.

10 Report the worst value of the pulse width as the final test result.

Expected/Observable Results: Generation of an eye diagram for the LPDDR4 data CA cycle and loading of a default test mask pattern.

The test will show a fail status if the total failed waveforms is greater than zero.

Set the statistic measurement to ON to get the worst width measurement of the CA signal and the worst result will be reported.

6 Eye Diagram Tests Group

Overview

The following group of tests pertains to the debug tool tests that enable user to perform evaluation and signal debugging on the signal(s) of interest.

Read/Write Eye Diagram Tests

tDIVW Margin

Mode Supported: DDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signals (supported by Data Strobe Signals)

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = DQ Signals.
- Supporting Pin = DQS Signals.

References: There is no limit found for this test.

Test Overview: The purpose of this test is to automate all the required setup procedures required in order to generate an eye diagram for the DDR4 data WRITE cycle.

The additional feature of having a mask test is allow users to perform evaluations and debugging on the eye diagram created.

Procedure:

1 Calculate initial time scale value based on selected DDR4 speed grade options.

2 Calculate number of sampling points according to the time scale value.

3 Check for valid DQS input test signals by verifying its frequency and amplitude values.

4 Set up the oscilloscope:

  a Using UDF methodology to separate Write burst and return the filtered DQS signals as recovered clock for eye folding later.

  b Set up measurement threshold values for the DQx channel and the DQSx channel input.

  c Set up vertical scale values for DQx channel and DQSx channel input.

  d Turn ON Color Grade Display option.

  e Identify the X1 value for re-adjustment of selected test mask.

  f Set up Mask Test. (Load default Test Mask on screen)

  g Set up Clock Recovery on SDA.

  : Explicit clock, Source = DQS, Rise/Fall Edge

  h Turn ON Real Time Eye on SDA.

5 Perform Mask Testing:
   a Set the termination condition of the mask test to 'Waveforms' with the number of waveforms to be acquired.
   b Start mask test with default Test Mask first.
6 Loop until number of required waveforms is acquired.
7 Get or Acquire Vcent Value. There is option for Vcent derivation depending on "Vcent Evaluation Mode" configuration. If "Vcent Evaluation Mode" option set to be "User defined Vcent" then the value of Vcent will follow the value of "User Defined Vcent" configuration. If "Vcent Evaluation Mode" option set to be "Widest eye opening level" then Application will evaluate VCent value based on the level of widest eye opening on eye diagram.
8 The detail procedure of "Widest eye opening level" is below;
   a Measure the Vmin and Vmax.
   b The Vcent level search range from 40% to 60% of the level between Vmin and Vmax. Mathematically, VcentSearchStart= Vmin + 0.6 * (Vmax - Vmin); and , VcentSearchEnd= Vmin + 0.4 * (Vmax - Vmin);
   c Find the eye opening at VcentSearchStart then store the level and eye opening width. Perform the same for VcentSearchStart+5mV, VcentSearchStart+10mV, VcentSearchStart+15mV.......... VcentSearchEnd. Find the level of widest eye opening from stored eye opening width measurement. Eventually assign found level as Vcent.
9 Adjust the default rectangular Test Mask as below;
   - Upper Mask Level: Vcent +0.5xCompliance_vDivw_Value= Vcent +0.5x136mV= Vcent +68mV
   - Lower Mask Level: Vcent -0.5xCompliance_vDivw_Value= Vcent -0.5x136mV= Vcent -68mV
   - Right Mask Position:TimePosition+0.5xCompliance_tDivw_Value= TimePosition+0.5xUI
   - Left Mask Position: TimePosition-0.5xCompliance_tDivw_Value= TimePosition-0.5xUI
10 Perform the tDIVW margin measurement on upper right corner of the mask. The detail procedure as below;
   a Setup histogram window;
      - Left window: 0s (Center position of Eye/Mask)
      - Right window: Right side of the grid.
      - Upper window: Top Level of Mask.
      - Lower window: Top Level of Mask.
   b Perform horizontal Histogram Min.
   c tDIVW margin upper right = 100% * (Histogram_Min -0.5 x Compliance_tDivw_Value) / (0.5 x Compliance_tDivw_Value).

11 Perform the tDIVW margin measurement on upper left corner of the mask. The detail procedure as below;
   a Setup histogram window;
      - Left window: Left side of the grid.
      - Right window: 0s (Center position of Eye/Mask)
      - Upper window: Top Level of Mask.
      - Lower window: Top Level of Mask.
   b Perform horizontal Histogram Max.
   c tDIVW margin upper left= 100% * (-0.5 x Compliance_tDivw_Value – Histogram_Max) / (0.5 x Compliance_tDivw_Value).
12 Perform the tDIVW margin measurement on lower right corner of the mask. The detail procedure as below;
   a Setup histogram window;
      - Left window: 0s (Center position of Eye/Mask)
      - Right window: Right side of the grid.
      - Upper window: Bottom Level of Mask.
      - Lower window: Bottom Level of Mask.
   b Perform horizontal Histogram Min.
   c tDIVW margin lower right = 100% * (Histogram_Min -0.5 x Compliance_tDivw_Value) / (0.5 x Compliance_tDivw_Value).
13 Perform the tDIVW margin measurement on lower left corner of the mask. The detail procedure as below;
   a Setup histogram window;
      - Left window: Left side of the grid.
      - Right window: 0s (Center position of Eye/Mask)
      - Upper window: Bottom Level of Mask.
      - Lower window: Bottom Level of Mask.
   b Perform horizontal Histogram Max.
   c tDIVW margin lower left= 100% * (-0.5 x Compliance_tDivw_Value – Histogram_Max) / (0.5 x Compliance_tDivw_Value).
14 Take minimum result between tDIVW margin upper left, tDIVW margin upper right, tDIVW margin lower left and tDIVW margin lower right as worst result.
15 Report worst result.

Expected/Observable Results: Generation of an eye diagram for the DDR4 data WRITE cycle and loading of a default test mask pattern.

The calculated tDIVW Margin shall meet the user defined limit.

vDIVW Margin

Mode Supported: DDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signals (supported by Data Strobe Signals)

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = DQ Signals.
- Supporting Pin = DQS Signals.

References: There is no limit found for this test.

Test Overview: The purpose of this test is to automate all the required setup procedures required in order to generate an eye diagram for the DDR4 data WRITE cycle.

The additional feature of having a mask test is allow users to perform evaluations and debugging on the eye diagram created.

Procedure:

1. Calculate initial time scale value based on selected DDR4 speed grade options.
2. Calculate number of sampling points according to the time scale value.
3. Check for valid DQS input test signals by verifying its frequency and amplitude values.
4. Set up the oscilloscope:
   - **a** Using UDF methodology to separate Write burst and return the filtered DQS signals as recovered clock for eye folding later.
   - **b** Set up measurement threshold values for the DQx channel and the DQSx channel input.
   - **c** Set up vertical scale values for DQx channel and DQSx channel input.
   - **d** Turn ON Color Grade Display option.
   - **e** Identify the X1 value for re-adjustment of selected test mask.
   - **f** Set up Mask Test. (Load default Test Mask on screen)
   - **g** Set up Clock Recovery on SDA.

     : Explicit clock, Source = DQS, Rise/Fall Edge
   - **h** Turn ON Real Time Eye on SDA.

5 Perform Mask Testing:

  a Set the termination condition of the mask test to 'Waveforms' with the number of waveforms to be acquired.

  b Start mask test with default Test Mask first.

6 Loop until number of required waveforms is acquired.

7 Get or Acquire Vcent Value. There is option for Vcent derivation depending on "Vcent Evaluation Mode" configuration. If "Vcent Evaluation Mode" option set to be "User defined Vcent" then the value of Vcent will follow the value of "User Defined Vcent" configuration. If "Vcent Evaluation Mode" option set to be "Widest eye opening level" then Application will evaluate VCent value based on the level of widest eye opening on eye diagram.

8 The detail procedure of "Widest eye opening level" is below;

  a Measure the Vmin and Vmax.

  b The Vcent level search range from 40% to 60% of the level between Vmin and Vmax. Mathematically, VcentSearchStart= Vmin + 0.6 * (Vmax - Vmin); and , VcentSearchEnd= Vmin + 0.4 * (Vmax - Vmin);

  c Find the eye opening at VcentSearchStart then store the level and eye opening width. Perform the same for VcentSearchStart+5mV, VcentSearchStart+10mV, VcentSearchStart+15mV.......... VcentSearchEnd. Find the level of widest eye opening from stored eye opening width measurement. Eventually assign found level as Vcent.

9 Adjust the default rectangular Test Mask as below;

  - Upper Mask Level: Vcent +0.5xCompliance_vDivw_Value= Vcent +0.5x136mV= Vcent +68mV
  - Lower Mask Level: Vcent -0.5xCompliance_vDivw_Value= Vcent -0.5x136mV= Vcent -68mV
  - Right Mask Position:TimePosition+0.5xCompliance_tDivw_Value= TimePosition+0.5xUI
  - Left Mask Position: TimePosition-0.5xCompliance_tDivw_Value= TimePosition-0.5xUI

10 Perform the vDIVW margin measurement on upper side of the mask. The detail procedure as below;

  a Setup histogram window;

    - Left window: -0.5xCompliance_tDivw_Value
    - Right window: 0.5xCompliance_tDivw_Value
    - Upper window: found Vmax of DQ signal.
    - Lower window: found Vcent.

  b Perform Histogram Min.

  c vDIVW margin upper= 100% * (Histogram Min – Upper Level Of Mask)/ (0.5xCompliance_vDivw_Value).

11 Perform the vDIVW margin measurement on lower side of the mask. The detail procedure as below;

   a Setup histogram window;
      - Left window: -0.5xCompliance_tDivw_Value
      - Right window: 0.5xCompliance_tDivw_Value
      - Upper window: found Vcent.
      - Lower window: found Vmin of DQ signal.

   b Perform Histogram Max.

   c vDIVW margin lower= 100% * (Bottom Level Of Mask - Histogram Max)/ (0.5xCompliance_vDivw_Value).

12 Take minimum result between vDIVW margin upper and vDIVW margin lower as worst result.

13 Report worst result.

Expected/Observable Results: Generation of an eye diagram for the DDR4 data WRITE cycle and loading of a default test mask pattern.

The calculated vDIVW Margin shall meet the user defined limit.

User Defined Real-Time Eye Diagram Test for Read Cycle

Mode Supported: DDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:
- Data Signals (supported by Data Strobe Signals)

Required Signals: Needed to perform this test on oscilloscope:
- Pin Under Test, PUT = DQ Signals.
- Supporting Pin = DQS Signals.

References: There is no available test specification on eye testing in JEDEC specifications. Mask testing is definable by the customers for their evaluation tests usage.

Test Overview: The purpose of this test is to automate all the required setup procedures required in order to generate an eye diagram for the DDR4 data READ cycle.

The additional feature of having a mask test is allow users to perform evaluations and debugging on the eye diagram created.

Procedure:

1. Calculate initial time scale value based on selected DDR4 speed grade options.
2. Calculate number of sampling points according to the time scale value.
3. Check for valid DQS input test signals by verifying its frequency and amplitude values.
4. Set up the oscilloscope:
   a. Using UDF methodology to separate Read burst and return the filtered DQS signals as recovered clock for eye folding later.
   b. Set up measurement threshold values for the DQx channel and the DQSx channel input.
   c. Set up vertical scale values for DQx channel and DQSx channel input.
   d. Turn ON Color Grade Display option.
   e. Identify the X1 value for re-adjustment of selected test mask.
   f. Set up Mask Test. (Load default Test Mask on screen)
   g. Set up Clock Recovery on SDA.

      : Explicit clock, Source = DQS, Rise/Fall Edge
   h. Turn ON Real Time Eye on SDA.
5. Perform Mask Testing:
   a. Set the termination condition of the mask test to 'Waveforms' with the number of waveforms to be acquired.
   b. Start mask test.
6. Loop until number of required waveforms is acquired.
7. Return total failed waveforms as a test result.

Expected/Observable Results: Generation of an eye diagram for the DDR4 data READ cycle and loading of a default test mask pattern.

The test will show a fail status if the total failed waveforms is greater than 0.

User Defined Real-Time Eye Diagram Test for Write Cycle

Mode Supported: DDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signals (supported by Data Strobe Signals)

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = DQ Signals.
- Supporting Pin = DQS Signals.

References: There is no available test specification on eye testing in JEDEC specifications. Mask testing is definable by the customers for their evaluation tests usage.

Test Overview: The purpose of this test is to automate all the required setup procedures required in order to generate an eye diagram for the DDR4 data WRITE cycle.

The additional feature of having a mask test is allow users to perform evaluations and debugging on the eye diagram created.

Procedure:

1. Calculate initial time scale value based on selected DDR4 speed grade options.
2. Calculate number of sampling points according to the time scale value.
3. Check for valid DQS input test signals by verifying its frequency and amplitude values.
4. Set up the oscilloscope:
   a. Using UDF methodology to separate Write burst and return the filtered DQS signals as recovered clock for eye folding later.
   b. Set up measurement threshold values for the DQx channel and the DQSx channel input.
   c. Set up vertical scale values for DQx channel and DQSx channel input.
   d. Turn ON Color Grade Display option.
   e. Identify the X1 value for re-adjustment of selected test mask.
   f. Set up Mask Test. (Load default Test Mask on screen)
   g. Set up Clock Recovery on SDA.

      : Explicit clock, Source = DQS, Rise/Fall Edge
   h. Turn ON Real Time Eye on SDA.
5. Perform Mask Testing:
   a. Set the termination condition of the mask test to 'Waveforms' with the number of waveforms to be acquired.
   b. Start mask test.
6. Loop until number of required waveforms is acquired.
7. Return total failed waveforms as a test result.

Expected/Observable Results: Generation of an eye diagram for the DDR4 data WRITE cycle and loading of a default test mask pattern.

The test will show a fail status if the total failed waveforms is greater than 0.

tQW_total Test for Read Cycle

Mode Supported: LPDDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signals (supported by Data Strobe Signals)

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = DQ Signals.
- Supporting Pin = DQS Signals.

References:

Specifications document	Section#	Table#
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.5	Table 92

Table 92 — Read output timings

Parameter	Symbol	LPDDR4-1600/1867		LPDDR4-2133/2400		LPDDR4-3200		LPDDR4-4266		Units*	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data Timing											
DQS_t,DQS_c to DQ Skew total, per group, per access (DBIDisabled)	tDQSQ	-	0.18	-	0.18	-	0.18	-	0.18	UI	1
DQ output hold time total from DQS_t, DQS_c (DBI-Disabled)	tQH	min(tQSH, tQSL)	-	min(tQSH, tQSL)	-	min(tQSH, tQSL)	-	min(tQSH, tQSL)	-	UI	1
DQ output window time total, per pin (DBI-Disabled)	tQW_total	0.75	-	0.73	-	0.7	-	0.7	-	UI	1,4
DQ output window time deterministic, per pin (DBIDisabled)	tQW_dj	TBD	-	TBD	-	-	TBD	-	TBD	UI	1,4,3
DQS_t,DQS_c to DQ Skew total,per group, per access (DBI-Enabled)	tDQSQ_DBI	-	TBD	-	TBD	-	TBD	-	TBD	UI	1
DQ output hold time total from DQS_t, DQS_c (DBI-Enabled)	tQH_DBI	min(tQSH_DBI, tQSL_DBI)	-	min(tQSH_DBI, tQSL_DBI)	-	min(tQSH_DBI, tQSL_DBI)	-	min(tQSH_DBI, tQSL_DBI)	TBD	UI	1
DQ output window time total, per pin (DBI-Enabled)	tQW_total_DBI	TBD	-	TBD	-	-	TBD	-	TBD	UI	1,4

Test Overview: The purpose of this test is to automate all the required setup procedures required in order to generate an eye diagram for the LPDDR4 data READ cycle.

The additional feature of having a mask test is allow users to perform evaluations and debugging on the eye diagram created.

Procedure:

1 Calculate initial time scale value based on selected LPDDR4 speed grade options.

2 Calculate number of sampling points according to the time scale value.

3 Check for valid DQS input test signals by verifying its frequency and amplitude values.

4 Set up the oscilloscope:

   a Using UDF methodology to separate Write burst and return the filtered DQS signals as recovered clock for eye folding later.

   b Set up measurement threshold values for the DQx channel and the DQSx channel input.

   c Set up vertical scale values for DQx channel and DQSx channel input.

   d Turn ON Color Grade Display option.

   e Identify the X1 value for re-adjustment of selected test mask.

   f Set up Mask Test. (Load default Test Mask on screen)

   g Set up Clock Recovery on SDA.

   : Explicit clock, Source = DQS, Rise/Fall Edge

   h Turn ON Real Time Eye on SDA.

5 Perform Mask Testing:

   a Set the termination condition of the mask test to 'Waveforms' with the number of waveforms to be acquired.

   b Start mask test with default Test Mask first.

6 Loop until number of required waveforms is acquired.

7 Get or Acquire Vcent value. There is an option for Vcent derivation depending on the "Vcent Evaluation Mode" configuration. If the "Vcent Evaluation Mode" option is set to be "User defined Vcent", then the value of Vcent will follow the value of the "User Defined Vcent" configuration. If the "Vcent Evaluation Mode" option is set to be "Widest eye opening level", then the application will evaluate the VCent value based on the level of widest eye opening on eye diagram.

8 The detailed procedure of "Widest eye opening level" is:

   a Measure the Vmin and Vmax.

   b The Vcent level search range from 40% to 60% of the level between Vmin and Vmax. Mathematically, VcentSearchStart= Vmin + 0.6 * (Vmax - Vmin); and , VcentSearchEnd= Vmin + 0.4 * (Vmax - Vmin).

   c Find the eye opening at VcentSearchStart; then, store the level and eye opening width. Perform the same for VcentSearchStart+5mV, VcentSearchStart+10mV, VcentSearchStart+15mV.......... VcentSearchEnd. Find the level of widest eye opening from stored eye opening width measurement. Eventually assign found level as Vcent.

9 Adjust the default rectangular Test Mask:

- Upper Mask Level: Vcent +0.5xCompliance_vQw_Value= Vcent +0.5x136mV= Vcent +68mV
- Lower Mask Level: Vcent -0.5xCompliance_vQw_Value= Vcent -0.5x136mV= Vcent -68mV
- Right Mask Position:TimePosition+0.5xTime_Range_Value
- Left Mask Position: TimePosition-0.5xTime_Range_Value

10 Perform the tQW measurement on upper right corner of the mask. The detailed procedure is:

a Set up histogram window:

- Left window: 0s (Center position of Eye/Mask).
- Right window: Right side of the grid.
- Upper window: Top Level of Mask.
- Lower window: Top Level of Mask.

b Perform horizontal Histogram Min.

c tQW upper right = (CurtQW_time - (TimePos + tQW_Compliance / 2)) / (tQW_Compliance / 2) * 100%.

11 Perform the tQW measurement on upper left corner of the mask. The detailed procedure is:

a Set up histogram window:

- Left window: Left side of the grid.
- Right window: 0s (Center position of Eye/Mask).
- Upper window: Top Level of Mask.
- Lower window: Top Level of Mask.

b Perform horizontal Histogram Max.

c tQW upper left= ((TimePos - tQW_Compliance / 2) - CurtQW_time) / (tQW_Compliance / 2) * 100%.

12 Perform the tQW measurement on lower right corner of the mask. The detailed procedure is:

a Set up histogram window:

- Left window: 0s (Center position of Eye/Mask).
- Right window: Right side of the grid.
- Upper window: Bottom Level of Mask.
- Lower window: Bottom Level of Mask.

b Perform horizontal Histogram Min.

c tQW lower right = (CurtQW_time - (TimePos + tQW_Compliance / 2)) / (tQW_Compliance / 2) * 100%.

13 Perform the tQW measurement on lower left corner of the mask. The detailed procedure is:

  a Set up histogram window:
    - Left window: Left side of the grid.
    - Right window: 0s (Center position of Eye/Mask).
    - Upper window: Bottom Level of Mask.
    - Lower window: Bottom Level of Mask.

  b Perform horizontal Histogram Max.

  c tQW lower left= ((TimePos - tQW_Compliance / 2) - CurtQW_time) / (tQW_Compliance / 2) * 100%.

14 Take minimum result between tQW margin upper left, tQW margin upper right, tQW margin lower left and tQW margin lower right as worst result.

15 Report worst result.

Expected/Observable Results: Generation of an eye diagram for the LPDDR4 data READ cycle and loading of a default test mask pattern.

The test will show a fail status if the total failed waveform is greater than 0 and report the tQW_top, tQW_bottom and tQW_min.

tQW_total_DBI Test for Read Cycle

Mode Supported: LPDDR4

Signal cycle of interest: READ

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signals (supported by Data Strobe Signals)

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = DQ Signals.
- Supporting Pin = DQS Signals.

References: There is no available test specification on eye testing in JEDEC specifications. Mask testing is definable by the customers for their evaluation tests usage.

Test Overview: The purpose of this test is to automate all the required setup procedures required in order to generate an eye diagram for the LPDDR4 data READ cycle.

The additional feature of having a mask test is allow users to perform evaluations and debugging on the eye diagram created.

Procedure:

1. Calculate initial time scale value based on selected LPDDR4 speed grade options.
2. Calculate number of sampling points according to the time scale value.
3. Check for valid DQS input test signals by verifying its frequency and amplitude values.
4. Set up the oscilloscope:
   a. Using UDF methodology to separate Write burst and return the filtered DQS signals as recovered clock for eye folding later.
   b. Set up measurement threshold values for the DQx channel and the DQSx channel input.
   c. Set up vertical scale values for DQx channel and DQSx channel input.
   d. Turn ON Color Grade Display option.
   e. Identify the X1 value for re-adjustment of selected test mask.
   f. Set up Mask Test. (Load default Test Mask on screen)
   g. Set up Clock Recovery on SDA.

      : Explicit clock, Source = DQS, Rise/Fall Edge
   h. Turn ON Real Time Eye on SDA.
5. Perform Mask Testing:
   a. Set the termination condition of the mask test to 'Waveforms' with the number of waveforms to be acquired.
   b. Start mask test with default Test Mask first.
6. Loop until number of required waveforms is acquired.
7. Get or Acquire Vcent value. There is an option for Vcent derivation depending on the "Vcent Evaluation Mode" configuration. If the "Vcent Evaluation Mode" option is set to be "User defined Vcent", then the value of Vcent will follow the value of the "User Defined Vcent" configuration. If the "Vcent Evaluation Mode" option is set to be "Widest eye opening level", then the application will evaluate the VCent value based on the level of widest eye opening on eye diagram.
8. The detailed procedure of "Widest eye opening level" is:
   a. Measure the Vmin and Vmax.
   b. The Vcent level search range from 40% to 60% of the level between Vmin and Vmax. Mathematically, VcentSearchStart= Vmin + 0.6 * (Vmax - Vmin); and , VcentSearchEnd= Vmin + 0.4 * (Vmax - Vmin).
   c. Find the eye opening at VcentSearchStart; then, store the level and eye opening width. Perform the same for VcentSearchStart+5mV, VcentSearchStart+10mV, VcentSearchStart+15mV.......... VcentSearchEnd. Find the level of widest eye opening from stored eye opening width measurement. Eventually assign found level as Vcent.
9. Adjust the default rectangular Test Mask:

- Upper Mask Level: Vcent +0.5xCompliance_vDivw_Value= Vcent +0.5x136mV= Vcent +68mV
- Lower Mask Level: Vcent -0.5xCompliance_vDivw_Value= Vcent -0.5x136mV= Vcent -68mV
- Right Mask Position:TimePosition+0.5xCompliance_tDivw_Value= TimePosition+0.5xUI
- Left Mask Position: TimePosition-0.5xCompliance_tDivw_Value= TimePosition-0.5xUI

10 Perform the tQW measurement on upper right corner of the mask. The detailed procedure is:

a Set up histogram window:

- Left window: 0s (Center position of Eye/Mask).
- Right window: Right side of the grid.
- Upper window: Top Level of Mask.
- Lower window: Top Level of Mask.

b Perform horizontal Histogram Min.

c tQW upper right = (CurtQW_time - (TimePos + tQW_Compliance / 2)) / (tQW_Compliance / 2) * 100%.

11 Perform the tQW measurement on upper left corner of the mask. The detailed procedure is:

a Set up histogram window:

- Left window: Left side of the grid.
- Right window: 0s (Center position of Eye/Mask).
- Upper window: Top Level of Mask.
- Lower window: Top Level of Mask.

b Perform horizontal Histogram Max.

c tQW upper left= ((TimePos - tQW_Compliance / 2) - CurtQW_time) / (tQW_Compliance / 2) * 100%.

12 Perform the tQW measurement on lower right corner of the mask. The detailed procedure is:

a Set up histogram window:

- Left window: 0s (Center position of Eye/Mask).
- Right window: Right side of the grid.
- Upper window: Bottom Level of Mask.

- Lower window: Bottom Level of Mask.

b Perform horizontal Histogram Min.

c tQW lower right = (CurtQW_time - (TimePos + tQW_Compliance / 2)) / (tQW_Compliance / 2) * 100%.

13 Perform the tQW measurement on lower left corner of the mask. The detailed procedure is:

a Set up histogram window:

- Left window: Left side of the grid.
- Right window: 0s (Center position of Eye/Mask).
- Upper window: Bottom Level of Mask.
- Lower window: Bottom Level of Mask.

b Perform horizontal Histogram Max.

c tQW lower left= ((TimePos - tQW_Compliance / 2) - CurtQW_time) / (tQW_Compliance / 2) * 100%.

14 Take minimum result between tQW margin upper left, tQW margin upper right, tQW margin lower left and tQW margin lower right as worst result.

15 Report worst result.

Expected/Observable Results: Generation of an eye diagram for the LPDDR4 data READ cycle and loading of a default test mask pattern.

The test will show a fail status if the total failed waveforms is greater than 0.

tDQS2DQ Test for Write Cycle

Mode Supported: LPDDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signals (supported by Data Strobe Signals)

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = DQ Signals.
- Supporting Pin = DQS Signals.

References:

Specifications document	Section#	Table#
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.6	Table 94

Table 94 — DRAM DQs In Receive Mode

Symbol	Parameter	1600/1867A		2133/2400		3200		4266		Unit	NOTE
		min	max	min	max	min	max	min	max		
VdIVW_total	Rx Mask voltage - p-p total	-	140	-	140	-	140	-	120	mV	1,2,3,5
TdIVW_total	Rx timing window total (At VdIVW voltage levels)	-	0.22	-	0.22	-	0.25	-	0.25	UI*	1,2,4,5
TdIVW_1bit	Rx timing window 1 bit toggle (At VdIVW voltage levels)	-	TBD	-	TBD	-	TBD	-	TBD	UI*	1,2,4, 5,14
VIHL_AC	DQ AC input pulse amplitude pk-pk	180	-	180	-	180	-	170	-	mV	7,15
TdIPW DQ	Input pulse width (At Vcent_DQ)	0.45		0.45		0.45		0.45		UI*	8
tDQS2DQ	DQ to DQS offset	200	800	200	800	200	800	200	800	ps	9
tDQDQ	DQ to DQ offset	-	30	-	30	-	30	-	30	ps	10
tDQS2DQ_temp	DQ to DQS offset temperature variation	-	0.6	-	0.6	-	0.6	-	0.6	ps/°C	11
tDQS2DQ_volt	DQ to DQS offset voltage variation	-	33	-	33	-	33	-	33	ps/50mV	12
SRIN_dIVW	Input Slew Rate over VdIVW_total	1	7	1	7	1	7	1	7	V/ns	13

* UI = tCK(avg)min/2

A The following Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. For example the TcIVW(ps) = 450ps at or below 1333 operating frequencies.

Test Overview: The purpose of this test is to automate all the required setup procedures required in order to generate an eye diagram for the LPDDR4 data WRITE cycle.

The additional feature of having a mask test is allow users to perform evaluations and debugging on the eye diagram created.

Procedure:

1. Calculate initial time scale value based on selected LPDDR4 speed grade options.
2. Calculate number of sampling points according to the time scale value.
3. Check for valid DQS input test signals by verifying its frequency and amplitude values.

4 Set up the oscilloscope:

   a Using UDF methodology to separate Write burst and return the filtered DQS signals as recovered clock for eye folding later.

   b Set up measurement threshold values for the DQx channel and the DQSx channel input.

   c Set up vertical scale values for DQx channel and DQSx channel input.

   d Turn ON Color Grade Display option.

   e Identify the X1 value for re-adjustment of selected test mask.

   f Set up Mask Test. (Load default Test Mask on screen)

   g Set up Clock Recovery on SDA.

   : Explicit clock, Source = DQS, Rise/Fall Edge

   h Turn ON Real Time Eye on SDA.

5 Perform Mask Testing:

   a Set the termination condition of the mask test to 'Waveforms' with the number of waveforms to be acquired.

   b Start mask test with default Test Mask first.

6 Loop until number of required waveforms is acquired.

7 Get or Acquire Vcent value. There is an option for Vcent derivation depending on the "Vcent Evaluation Mode" configuration. If the "Vcent Evaluation Mode" option is set to be "User defined Vcent", then the value of Vcent will follow the value of the "User Defined Vcent" configuration. If the "Vcent Evaluation Mode" option is set to be "Widest eye opening level", then the application will evaluate the VCent value based on the level of widest eye opening on eye diagram.

8 The detailed procedure of "Widest eye opening level" is:

   a Measure the Vmin and Vmax.

   b The Vcent level search range from 40% to 60% of the level between Vmin and Vmax. Mathematically, VcentSearchStart= Vmin + 0.6 * (Vmax - Vmin); and , VcentSearchEnd= Vmin + 0.4 * (Vmax - Vmin).

   c Find the eye opening at VcentSearchStart; then, store the level and eye opening width. Perform the same for VcentSearchStart+5mV, VcentSearchStart+10mV, VcentSearchStart+15mV.......... VcentSearchEnd. Find the level of widest eye opening from stored eye opening width measurement. Eventually assign found level as Vcent.

   d TimePos = Query the current time position. TimeRange = Query current time range.

9 Perform the histogram measurement on left corner of the mask. The detailed procedure is:

   a Set up histogram window:

      - Left window: TimePos - 0.5 * TimeRange.

- Right window: TimePos.
- Upper window: VCENT + 5e-3.
- Lower window: VCENT - 5e-3.

b Perform horizontal Histogram Max and then the result assign to LeftSidePos.

10 Perform the histogram measurement on right corner of the mask. The detailed procedure is:

a Set up histogram window:

- Left window: TimePos.
- Right window: TimePos + 0.5 * TimeRange.
- Upper window: VCENT + 5e-3.
- Lower window: VCENT - 5e-3.

b Perform horizontal Histogram Min and then the result assign to RightSidePos.

11 New TimePos = (LeftSidePos + RightSidePos) / 2.

12 tDQS2DQ = TimePos – 0.

Expected/Observable Results: Generation of an eye diagram for the LPDDR4 data WRITE cycle and loading of a default test mask pattern.

The test will show a fail status if the total failed waveforms is greater than 0.

DQ VIHL(ac) Test for Write Cycle

Mode Supported: LPDDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signals (supported by Data Strobe Signals)

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = DQ Signals.
- Supporting Pin = DQS Signals.

References:

Specifications document	Section#	Table#
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.6	Table 94

Table 94 — DRAM DQs In Receive Mode

Symbol	Parameter	1600/1867[A]		2133/2400		3200		4266		Unit	NOTE
		min	max	min	max	min	max	min	max		
VdIVW_total	Rx Mask voltage - p-p total	-	140	-	140	-	140	-	120	mV	1,2,3,5
TdIVW_total	Rx timing window total (At VdIVW voltage levels)	-	0.22	-	0.22	-	0.25	-	0.25	UI*	1,2,4,5
TdIVW_1bit	Rx timing window 1 bit toggle (At VdIVW voltage levels)	-	TBD	-	TBD	-	TBD	-	TBD	UI*	1,2,4, 5,14
VIHL_AC	DQ AC input pulse amplitude pk-pk	180	-	180	-	180	-	170	-	mV	7,15
TdIPW DQ	Input pulse width (At Vcent_DQ)	0.45		0.45		0.45		0.45		UI*	8
tDQS2DQ	DQ to DQS offset	200	800	200	800	200	800	200	800	ps	9
tDQDQ	DQ to DQ offset	-	30	-	30	-	30	-	30	ps	10
tDQS2DQ_temp	DQ to DQS offset temperature variation	-	0.6	-	0.6	-	0.6	-	0.6	ps/°C	11
tDQS2DQ_volt	DQ to DQS offset voltage variation	-	33	-	33	-	33	-	33	ps/50mV	12
SRIN_dIVW	Input Slew Rate over VdIVW_total	1	7	1	7	1	7	1	7	V/ns	13

* UI = tCK(avg)min/2

A The following Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. For example the TcIVW(ps) = 450ps at or below 1333 operating frequencies.

Test Overview: The purpose of this test is to automate all the required setup procedures required in order to generate an eye diagram for the LPDDR4 data WRITE cycle.

The additional feature of having a mask test is allow users to perform evaluations and debugging on the eye diagram created.

Procedure:

1. Calculate initial time scale value based on selected LPDDR4 speed grade options.
2. Calculate number of sampling points according to the time scale value.
3. Check for valid DQS input test signals by verifying its frequency and amplitude values.
4. Set up the oscilloscope:
   - **a** Using UDF methodology to separate Write burst and return the filtered DQS signals as recovered clock for eye folding later.
   - **b** Set up measurement threshold values for the DQx channel and the DQSx channel input.
   - **c** Set up vertical scale values for DQx channel and DQSx channel input.
   - **d** Turn ON Color Grade Display option.
   - **e** Identify the X1 value for re-adjustment of selected test mask.
   - **f** Set up Mask Test. (Load default Test Mask on screen)
   - **g** Set up Clock Recovery on SDA.

     : Explicit clock, Source = DQS, Rise/Fall Edge
   - **h** Turn ON Real Time Eye on SDA.

5 Perform Mask Testing:
   a Set the termination condition of the mask test to 'Waveforms' with the number of waveforms to be acquired.
   b Start mask test with default Test Mask first.
6 Loop until number of required waveforms is acquired.
7 Get or Acquire Vcent value. There is an option for Vcent derivation depending on the "Vcent Evaluation Mode" configuration. If the "Vcent Evaluation Mode" option is set to be "User defined Vcent", then the value of Vcent will follow the value of the "User Defined Vcent" configuration. If the "Vcent Evaluation Mode" option is set to be "Widest eye opening level", then the application will evaluate the VCent value based on the level of widest eye opening on eye diagram.
8 The detailed procedure of "Widest eye opening level" is:
   a Measure the Vmin and Vmax.
   b The Vcent level search range from 40% to 60% of the level between Vmin and Vmax. Mathematically, VcentSearchStart= Vmin + 0.6 * (Vmax - Vmin); and , VcentSearchEnd= Vmin + 0.4 * (Vmax - Vmin).
   c Find the eye opening at VcentSearchStart; then, store the level and eye opening width. Perform the same for VcentSearchStart+5mV, VcentSearchStart+10mV, VcentSearchStart+15mV.......... VcentSearchEnd. Find the level of widest eye opening from stored eye opening width measurement. Eventually assign found level as Vcent.
9 Perform the histogram measurement on left corner of the mask. The detailed procedure is:
   a Set up histogram window:
      - Left window: TimePos - 0.5 * TimeRange.
      - Right window: TimePos.
      - Upper window: VCENT + 5e-3.
      - Lower window: VCENT - 5e-3.
   b Perform horizontal Histogram Max and then the result assign to LeftSidePos.
10 Perform the histogram measurement on right corner of the mask. The detailed procedure is:
   a Set up histogram window:
      - Left window: TimePos.
      - Right window: TimePos + 0.5 * TimeRange.
      - Upper window: VCENT + 5e-3.
      - Lower window: VCENT - 5e-3.
   b Perform horizontal Histogram Min and then the result assign to RightSidePos.

11 New TimePos = (LeftSidePos + RightSidePos) / 2.

12 VIHLScanStart = TimePos - (1 / DataRate) / 4.

13 VIHLScanEnd = TimePos + (1 / DataRate) / 4.

14 VIHLStepScan = 10e-12.

15 NoOfStepVIHL = 0.

16 CurTime = VIHLScanStart + NoOfStepVIHL * VIHLStepScan.

17 Perform the histogram measurement on top of the mask. The detailed procedure is:

   a Set up histogram window:
      - Left window: CurTime - VIHLStepScan / 2
      - Right window: CurTime + VIHLStepScan / 2
      - Upper window: VmaxDQ
      - Lower window: VCENT

   b Perform horizontal Histogram Max and then the result assign to LeftSidePos.

18 Perform the histogram measurement on bottom of the mask. The detailed procedure is:

   a Set up histogram window:
      - Left window: CurTime - VIHLStepScan / 2
      - Right window: CurTime + VIHLStepScan / 2
      - Upper window: VCENT
      - Lower window: VminDQ

19 Loop until VIHLScanEnd value.

20 Get MaxTop and MinBottom.

Expected/Observable Results: Generation of an eye diagram for the LPDDR4 data WRITE cycle and loading of a default test mask pattern.

The test will show a fail status if the total failed waveforms is greater than 0.

SRIN_diVW Test for Write Cycle

Mode Supported: LPDDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:
- Data Signals (supported by Data Strobe Signals)

Required Signals: Needed to perform this test on oscilloscope:
- Pin Under Test, PUT = DQ Signals.
- Supporting Pin = DQS Signals.

References:

Specifications document	Section#	Table#
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.6	Table 94

Table 94 — DRAM DQs In Receive Mode

Symbol	Parameter	1600/1867[A]		2133/2400		3200		4266		Unit	NOTE
		min	max	min	max	min	max	min	max		
VdIVW_total	Rx Mask voltage - p-p total	-	140	-	140	-	140	-	120	mV	1,2,3,5
TdIVW_total	Rx timing window total (At VdIVW voltage levels)	-	0.22	-	0.22	-	0.25	-	0.25	UI*	1,2,4,5
TdIVW_1bit	Rx timing window 1 bit toggle (At VdIVW voltage levels)	-	TBD	-	TBD	-	TBD	-	TBD	UI*	1,2,4, 5,14
VIHL_AC	DQ AC input pulse amplitude pk-pk	180	-	180	-	180	-	170	-	mV	7,15
TdIPW DQ	Input pulse width (At Vcent_DQ)	0.45		0.45		0.45		0.45		UI*	8
tDQS2DQ	DQ to DQS offset	200	800	200	800	200	800	200	800	ps	9
tDQDQ	DQ to DQ offset	-	30	-	30	-	30	-	30	ps	10
tDQS2DQ_temp	DQ to DQS offset temperature variation	-	0.6	-	0.6	-	0.6	-	0.6	ps/°C	11
tDQS2DQ_volt	DQ to DQS offset voltage variation	-	33	-	33	-	33	-	33	ps/50mV	12
SRIN_dIVW	Input Slew Rate over VdIVW_total	1	7	1	7	1	7	1	7	V/ns	13

* UI = tCK(avg)min/2

A The following Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. For example the TcIVW(ps) = 450ps at or below 1333 operating frequencies.

Test Overview: The purpose of this test is to automate all the required setup procedures required in order to generate an eye diagram for the LPDDR4 data WRITE cycle.

The additional feature of having a mask test is allow users to perform evaluations and debugging on the eye diagram created.

Procedure:

1. Calculate initial time scale value based on selected LPDDR4 speed grade options.
2. Calculate number of sampling points according to the time scale value.
3. Check for valid DQS input test signals by verifying its frequency and amplitude values.

4 Set up the oscilloscope:
   a Using UDF methodology to separate Write burst and return the filtered DQS signals as recovered clock for eye folding later.
   b Set up measurement threshold values for the DQx channel and the DQSx channel input.
   c Set up vertical scale values for DQx channel and DQSx channel input.
   d Turn ON Color Grade Display option.
   e Identify the X1 value for re-adjustment of selected test mask.
   f Set up Mask Test. (Load default Test Mask on screen)
   g Set up Clock Recovery on SDA.

   : Explicit clock, Source = DQS, Rise/Fall Edge
   h Turn ON Real Time Eye on SDA.
5 Perform Mask Testing:
   a Set the termination condition of the mask test to 'Waveforms' with the number of waveforms to be acquired.
   b Start mask test with default Test Mask first.
6 Loop until number of required waveforms is acquired.
7 Get or Acquire Vcent value. There is an option for Vcent derivation depending on the "Vcent Evaluation Mode" configuration. If the "Vcent Evaluation Mode" option is set to be "User defined Vcent", then the value of Vcent will follow the value of the "User Defined Vcent" configuration. If the "Vcent Evaluation Mode" option is set to be "Widest eye opening level", then the application will evaluate the VCent value based on the level of widest eye opening on eye diagram.
8 The detailed procedure of "Widest eye opening level" is:
   a Measure the Vmin and Vmax.
   b The Vcent level search range from 40% to 60% of the level between Vmin and Vmax. Mathematically, VcentSearchStart= Vmin + 0.6 * (Vmax - Vmin); and , VcentSearchEnd= Vmin + 0.4 * (Vmax - Vmin).
   c Find the eye opening at VcentSearchStart; then, store the level and eye opening width. Perform the same for VcentSearchStart+5mV, VcentSearchStart+10mV, VcentSearchStart+15mV.......... VcentSearchEnd. Find the level of widest eye opening from stored eye opening width measurement. Eventually assign found level as Vcent.
9 Adjust the default rectangular Test Mask:
   - Upper Mask Level: Vcent +0.5xCompliance_vDivw_Value= Vcent +0.5x136mV= Vcent +68mV
   - Lower Mask Level: Vcent -0.5xCompliance_vDivw_Value= Vcent -0.5x136mV= Vcent -68mV

- Right Mask Position:TimePosition+0.5xCompliance_tDivw_Value= TimePosition+0.5xUI
- Left Mask Position: TimePosition-0.5xCompliance_tDivw_Value= TimePosition-0.5xUI

10 Setup Slewrate rising measurement on DQ signal to get the SRIN_diVW rise time max and SRIN_diVW rise time min.

Expected/Observable Results: Generation of an eye diagram for the LPDDR4 data WRITE cycle and loading of a default test mask pattern.

The test will show a fail status if the total failed waveforms is greater than 0 and the SRIN_diVW rise time max and SRIN_diVW rise time min values are reported.

tDIVW Test for Write Cycle

Mode Supported: LPDDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signals (supported by Data Strobe Signals)

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = DQ Signals.
- Supporting Pin = DQS Signals.

References:

Specifications document	Section#	Table#
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.6	Table 94

Table 94 — DRAM DQs In Receive Mode

Symbol	Parameter	1600/1867[A]		2133/2400		3200		4266		Unit	NOTE
		min	max	min	max	min	max	min	max		
VdIVW_total	Rx Mask voltage - p-p total	-	140	-	140	-	140	-	120	mV	1,2,3,5
TdIVW_total	Rx timing window total (At VdIVW voltage levels)	-	0.22	-	0.22	-	0.25	-	0.25	UI*	1,2,4,5
TdIVW_1bit	Rx timing window 1 bit toggle (At VdIVW voltage levels)	-	TBD	-	TBD	-	TBD	-	TBD	UI*	1,2,4, 5,14
VIHL_AC	DQ AC input pulse amplitude pk-pk	180	-	180	-	180	-	170	-	mV	7,15
TdIPW DQ	Input pulse width (At Vcent_DQ)	0.45		0.45		0.45		0.45		UI*	8
tDQS2DQ	DQ to DQS offset	200	800	200	800	200	800	200	800	ps	9
tDQDQ	DQ to DQ offset	-	30	-	30	-	30	-	30	ps	10
tDQS2DQ_temp	DQ to DQS offset temperature variation	-	0.6	-	0.6	-	0.6	-	0.6	ps/°C	11
tDQS2DQ_volt	DQ to DQS offset voltage variation	-	33	-	33	-	33	-	33	ps/50mV	12
SRIN_dIVW	Input Slew Rate over VdIVW_total	1	7	1	7	1	7	1	7	V/ns	13

* UI = tCK(avg)min/2

A The following Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. For example the TcIVW(ps) = 450ps at or below 1333 operating frequencies.

Test Overview: The purpose of this test is to automate all the required setup procedures required in order to generate an eye diagram for the LPDDR4 data WRITE cycle.

The additional feature of having a mask test is allow users to perform evaluations and debugging on the eye diagram created.

Procedure:

1. Calculate initial time scale value based on selected LPDDR4 speed grade options.
2. Calculate number of sampling points according to the time scale value.
3. Check for valid DQS input test signals by verifying its frequency and amplitude values.
4. Set up the oscilloscope:
   - **a** Using UDF methodology to separate Write burst and return the filtered DQS signals as recovered clock for eye folding later.
   - **b** Set up measurement threshold values for the DQx channel and the DQSx channel input.
   - **c** Set up vertical scale values for DQx channel and DQSx channel input.
   - **d** Turn ON Color Grade Display option.
   - **e** Identify the X1 value for re-adjustment of selected test mask.
   - **f** Set up Mask Test. (Load default Test Mask on screen)
   - **g** Set up Clock Recovery on SDA.

     : Explicit clock, Source = DQS, Rise/Fall Edge
   - **h** Turn ON Real Time Eye on SDA.

5 Perform Mask Testing:

   a Set the termination condition of the mask test to 'Waveforms' with the number of waveforms to be acquired.

   b Start mask test with default Test Mask first.

6 Loop until number of required waveforms is acquired.

7 Get or Acquire Vcent value. There is an option for Vcent derivation depending on the "Vcent Evaluation Mode" configuration. If the "Vcent Evaluation Mode" option is set to be "User defined Vcent", then the value of Vcent will follow the value of the "User Defined Vcent" configuration. If the "Vcent Evaluation Mode" option is set to be "Widest eye opening level", then the application will evaluate the VCent value based on the level of widest eye opening on eye diagram.

8 The detailed procedure of "Widest eye opening level" is:

   a Measure the Vmin and Vmax.

   b The Vcent level search range from 40% to 60% of the level between Vmin and Vmax. Mathematically, VcentSearchStart= Vmin + 0.6 * (Vmax - Vmin); and , VcentSearchEnd= Vmin + 0.4 * (Vmax - Vmin).

   c Find the eye opening at VcentSearchStart; then, store the level and eye opening width. Perform the same for VcentSearchStart+5mV, VcentSearchStart+10mV, VcentSearchStart+15mV.......... VcentSearchEnd. Find the level of widest eye opening from stored eye opening width measurement. Eventually assign found level as Vcent.

9 Adjust the default rectangular Test Mask:

   - Upper Mask Level: Vcent +0.5xCompliance_vDivw_Value= Vcent +0.5x136mV= Vcent +68mV
   - Lower Mask Level: Vcent -0.5xCompliance_vDivw_Value= Vcent -0.5x136mV= Vcent -68mV
   - Right Mask Position:TimePosition+0.5xCompliance_tDivw_Value= TimePosition+0.5xUI
   - Left Mask Position: TimePosition-0.5xCompliance_tDivw_Value= TimePosition-0.5xUI

10 Perform the tDIVW margin measurement on upper right corner of the mask. The detailed procedure is:

   a Set up histogram window:

      - Left window: 0s (Center position of Eye/Mask).
      - Right window: Right side of the grid.
      - Upper window: Top Level of Mask.
      - Lower window: Top Level of Mask.

   b Perform horizontal Histogram Min.

   c tDIVW margin upper right = 100% * (Histogram_Min -0.5 x Compliance_tDivw_Value) / (0.5 x Compliance_tDivw_Value).

11 Perform the tDIVW margin measurement on upper left corner of the mask. The detailed procedure is:

   a Set up histogram window:

      - Left window: Left side of the grid.
      - Right window: 0s (Center position of Eye/Mask).
      - Upper window: Top Level of Mask.
      - Lower window: Top Level of Mask.

   b Perform horizontal Histogram Max.

   c tDIVW margin upper left= 100% * (-0.5 x Compliance_tDivw_Value – Histogram_Max) / (0.5 x Compliance_tDivw_Value).

12 Perform the tDIVW margin measurement on lower right corner of the mask. The detailed procedure is:

   a Set up histogram window:

      - Left window: 0s (Center position of Eye/Mask).
      - Right window: Right side of the grid.
      - Upper window: Bottom Level of Mask.
      - Lower window: Bottom Level of Mask.

   b Perform horizontal Histogram Min.

   c tDIVW margin lower right = 100% * (Histogram_Min -0.5 x Compliance_tDivw_Value) / (0.5 x Compliance_tDivw_Value).

13 Perform the tDIVW margin measurement on lower left corner of the mask. The detailed procedure is:

   a Set up histogram window:

      - Left window: Left side of the grid.
      - Right window: 0s (Center position of Eye/Mask).
      - Upper window: Bottom Level of Mask.
      - Lower window: Bottom Level of Mask.

   b Perform horizontal Histogram Max.

   c tDIVW margin lower left= 100% * (-0.5 x Compliance_tDivw_Value – Histogram_Max) / (0.5 x Compliance_tDivw_Value).

14 Take minimum result between tDIVW margin upper left, tDIVW margin upper right, tDIVW margin lower left and tDIVW margin lower right as worst result.

15 Report worst result.

Expected/Observable Results: Generation of an eye diagram for the DDR4 data WRITE cycle and loading of a default test mask pattern.

The calculated tDIVW Margin shall meet the user defined limit.

vDIVW Test for Write Cycle

Mode Supported: LPDDR4

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signals (supported by Data Strobe Signals)

Required Signals: Needed to perform this test on oscilloscope:

- Pin Under Test, PUT = DQ Signals.
- Supporting Pin = DQS Signals.

References:

Specifications document	Section#	Table#
LPDDR4 SDRAM Specification, JESD209-4, August 2014	10.6	Table 94

Table 94 — DRAM DQs In Receive Mode

Symbol	Parameter	1600/1867[A]		2133/2400		3200		4266		Unit	NOTE
		min	max	min	max	min	max	min	max		
VdIVW_total	Rx Mask voltage - p-p total	-	140	-	140	-	140	-	120	mV	1,2,3,5
TdIVW_total	Rx timing window total (At VdIVW voltage levels)	-	0.22	-	0.22	-	0.25	-	0.25	UI*	1,2,4,5
TdIVW_1bit	Rx timing window 1 bit toggle (At VdIVW voltage levels)	-	TBD	-	TBD	-	TBD	-	TBD	UI*	1,2,4, 5,14
VIHL_AC	DQ AC input pulse amplitude pk-pk	180	-	180	-	180	-	170	-	mV	7,15
TdIPW DQ	Input pulse width (At Vcent_DQ)	0.45		0.45		0.45		0.45		UI*	8
tDQS2DQ	DQ to DQS offset	200	800	200	800	200	800	200	800	ps	9
tDQDQ	DQ to DQ offset	-	30	-	30	-	30	-	30	ps	10
tDQS2DQ_temp	DQ to DQS offset temperature variation	-	0.6	-	0.6	-	0.6	-	0.6	ps/°C	11
tDQS2DQ_volt	DQ to DQS offset voltage variation	-	33	-	33	-	33	-	33	ps/50mV	12
SRIN_dIVW	Input Slew Rate over VdIVW_total	1	7	1	7	1	7	1	7	V/ns	13

* UI = tCK(avg)min/2

A The following Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. For example the TcIVW(ps) = 450ps at or below 1333 operating frequencies.

Test Overview: The purpose of this test is to automate all the required setup procedures required in order to generate an eye diagram for the LPDDR4 data WRITE cycle.

The additional feature of having a mask test is allow users to perform evaluations and debugging on the eye diagram created.

Procedure:

1. Calculate initial time scale value based on selected LPDDR4 speed grade options.
2. Calculate number of sampling points according to the time scale value.
3. Check for valid DQS input test signals by verifying its frequency and amplitude values.
4. Set up the oscilloscope:
   a. Using UDF methodology to separate Write burst and return the filtered DQS signals as recovered clock for eye folding later.
   b. Set up measurement threshold values for the DQx channel and the DQSx channel input.
   c. Set up vertical scale values for DQx channel and DQSx channel input.
   d. Turn ON Color Grade Display option.
   e. Identify the X1 value for re-adjustment of selected test mask.
   f. Set up Mask Test. (Load default Test Mask on screen)
   g. Set up Clock Recovery on SDA.

      : Explicit clock, Source = DQS, Rise/Fall Edge
   h. Turn ON Real Time Eye on SDA.
5. Perform Mask Testing:
   a. Set the termination condition of the mask test to 'Waveforms' with the number of waveforms to be acquired.
   b. Start mask test with default Test Mask first.
6. Loop until number of required waveforms is acquired.
7. Get or Acquire Vcent value. There is an option for Vcent derivation depending on the "Vcent Evaluation Mode" configuration. If the "Vcent Evaluation Mode" option is set to be "User defined Vcent", then the value of Vcent will follow the value of the "User Defined Vcent" configuration. If the "Vcent Evaluation Mode" option is set to be "Widest eye opening level", then the application will evaluate the VCent value based on the level of widest eye opening on eye diagram.
8. The detailed procedure of "Widest eye opening level" is:
   a. Measure the Vmin and Vmax.
   b. The Vcent level search range from 40% to 60% of the level between Vmin and Vmax. Mathematically, VcentSearchStart= Vmin + 0.6 * (Vmax - Vmin); and , VcentSearchEnd= Vmin + 0.4 * (Vmax - Vmin).
   c. Find the eye opening at VcentSearchStart; then, store the level and eye opening width. Perform the same for VcentSearchStart+5mV, VcentSearchStart+10mV, VcentSearchStart+15mV.......... VcentSearchEnd. Find the level of widest eye opening from stored eye opening width measurement. Eventually assign found level as Vcent.
9. Adjust the default rectangular Test Mask:

- Upper Mask Level: Vcent +0.5xCompliance_vDivw_Value= Vcent +0.5x136mV= Vcent +68mV
- Lower Mask Level: Vcent -0.5xCompliance_vDivw_Value= Vcent -0.5x136mV= Vcent -68mV
- Right Mask Position:TimePosition+0.5xCompliance_tDivw_Value= TimePosition+0.5xUI
- Left Mask Position: TimePosition-0.5xCompliance_tDivw_Value= TimePosition-0.5xUI

10 Perform the vDIVW margin measurement on upper side of the mask. The detailed procedure is:

a Set up histogram window:

- Left window: -0.5xCompliance_tDivw_Value.
- Right window: 0.5xCompliance_tDivw_Value.
- Upper window: found Vmax of DQ signal.
- Lower window: found Vcent.

b Perform horizontal Histogram Min.

c vDIVW margin upper= 100% * (Histogram Min – Upper Level Of Mask)/ (0.5xCompliance_vDivw_Value).

11 Perform the vDIVW margin measurement on lower side of the mask. The detailed procedure is:

a Set up histogram window:

- Left window: -0.5xCompliance_tDivw_Value.
- Right window: 0.5xCompliance_tDivw_Value.
- Upper window: found Vcent.
- Lower window: found Vmin of DQ signal.

b Perform Histogram Max.

c vDIVW margin lower= 100% * (Bottom Level Of Mask - Histogram Max)/ (0.5xCompliance_vDivw_Value).

12 Take minimum result between vDIVW margin upper and vDIVW margin lower as worst result.

13 Report worst result.

Expected/Observable Results: Generation of an eye diagram for the DDR4 data WRITE cycle and loading of a default test mask pattern.

The calculated vDIVW Margin shall meet the user defined limit.

A Reference

Documents

- Infiniium Oscilloscope Operation Manual
- Infiniium Oscilloscopes Programmer's Guide
- JESD79-4 document, September 2012
- JESD209-4 document, August 2014

Websites

- "http://www.elpida.com"
- "http://www.chips.ibm.com"
- "http://www.jedec.org"
- "http://www.intel.com"

Reference Figures from JESD79-4 Document

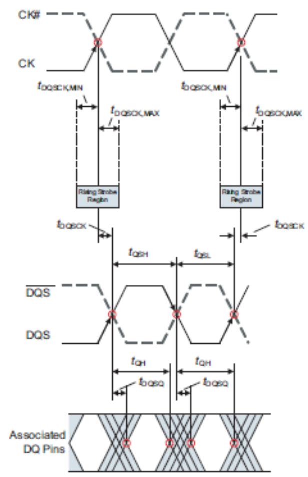


Figure 27 – READ Timing Definition

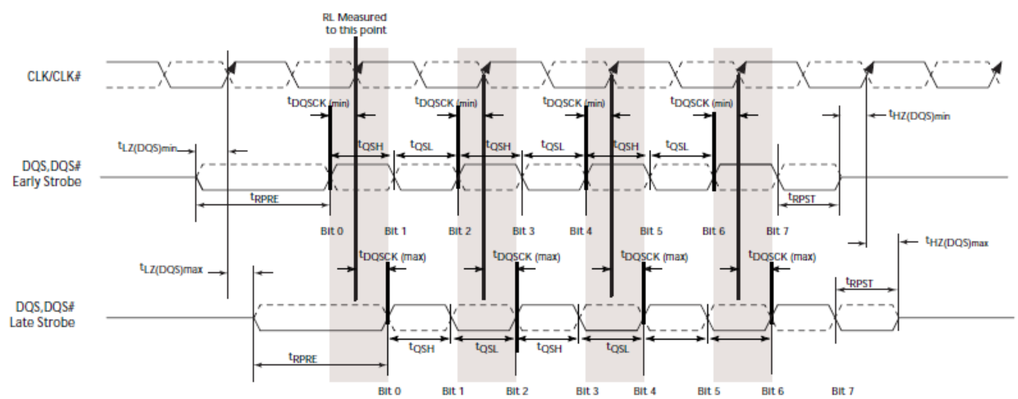


Figure 28 – Clock to Data Strobe Relationship

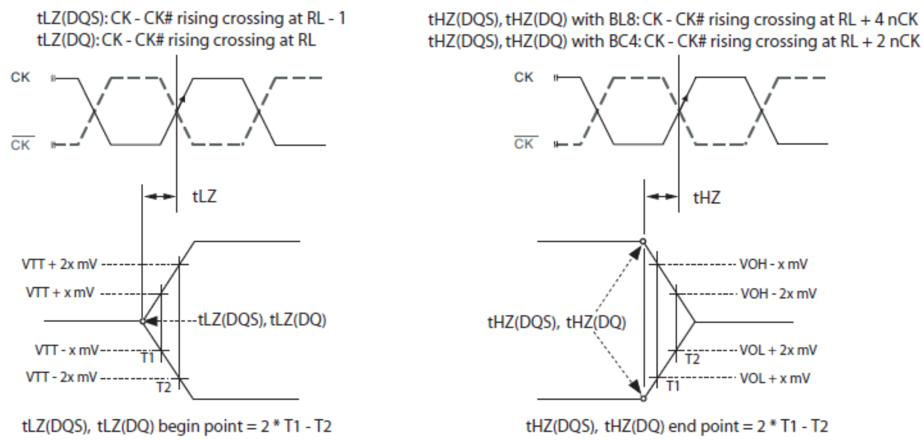


Figure 30 – tLZ and tHZ method for calculating transitions and endpoints

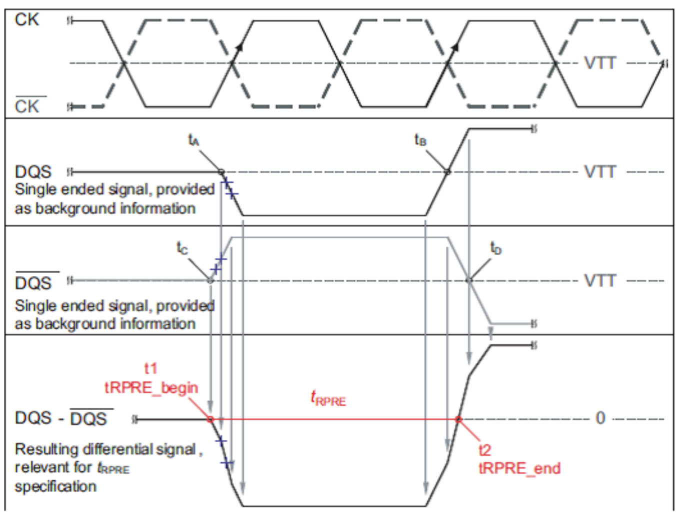


Figure 31 – Method for calculating tRPRE transitions and endpoints

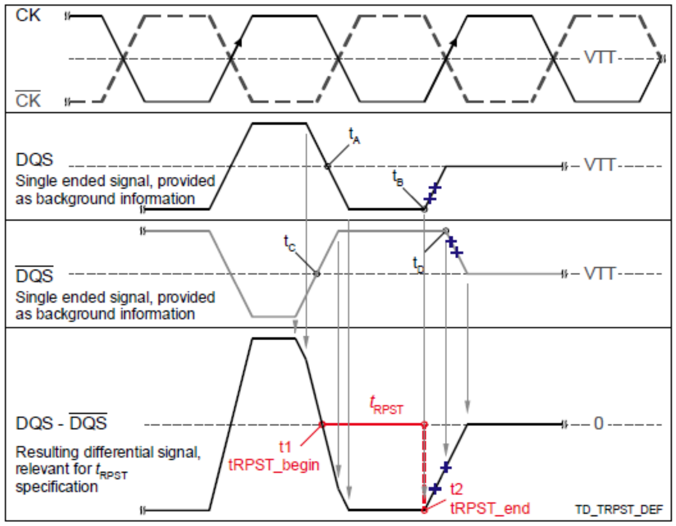


Figure 32 – Method for calculating tRPST transitions and endpoints

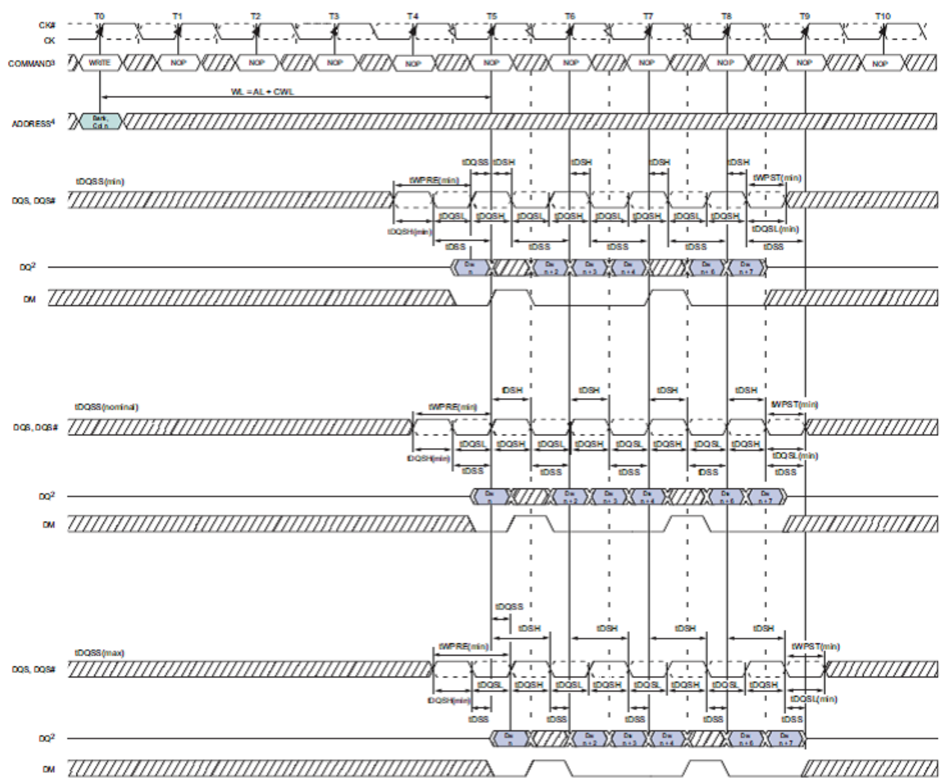


Figure 44 – Write Timing Definition and Parameters

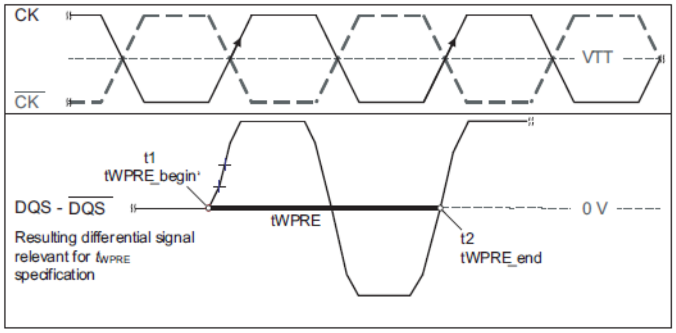


Figure 45 – Method for calculating tWPRE transitions and endpoints

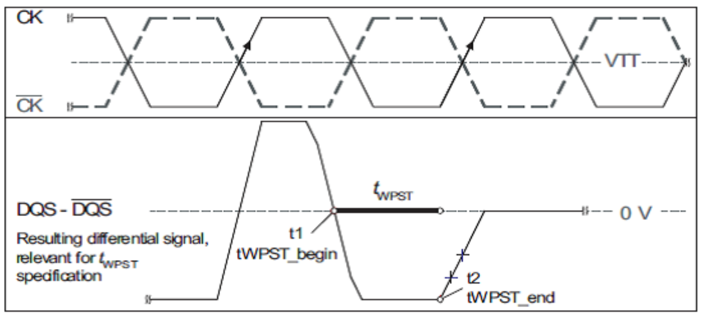


Figure 46 – Method for calculating tWPST transitions and endpoints

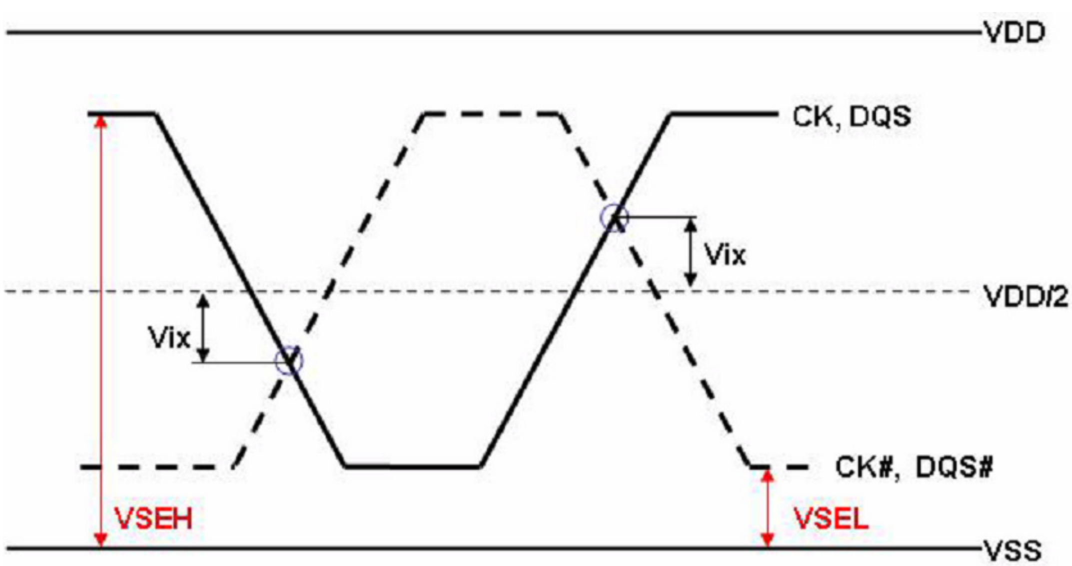


Figure 94 – Vix Definition

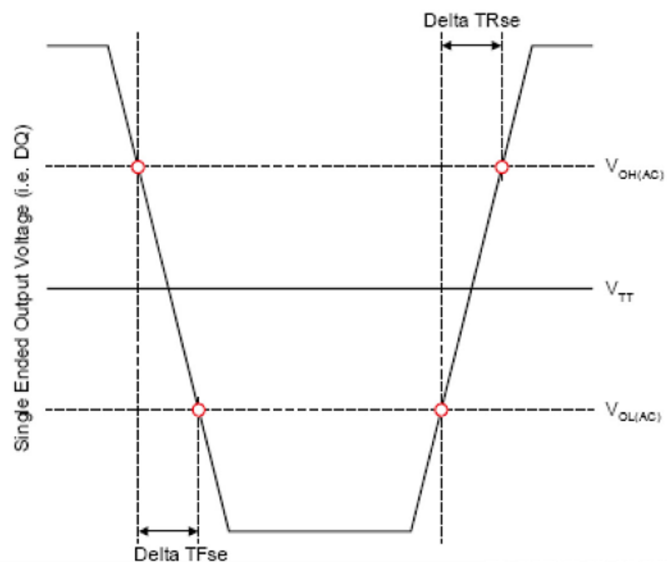


Figure 96 – Singe-ended Output Slew Rate Definition

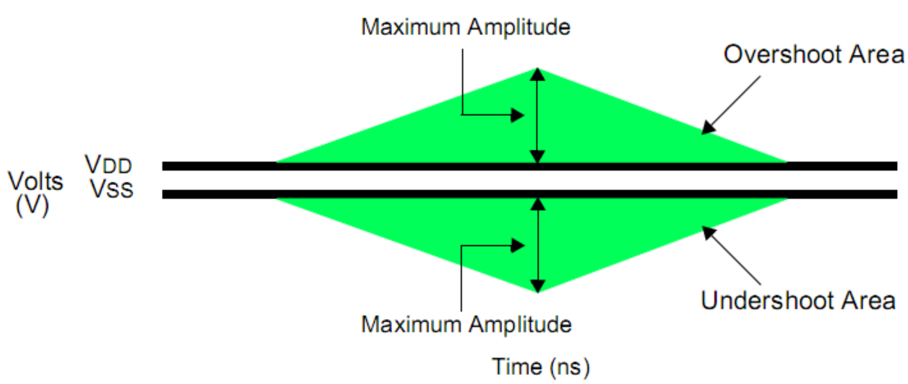


Figure 99 – Address and Control Overshoot and Undershoot Definition

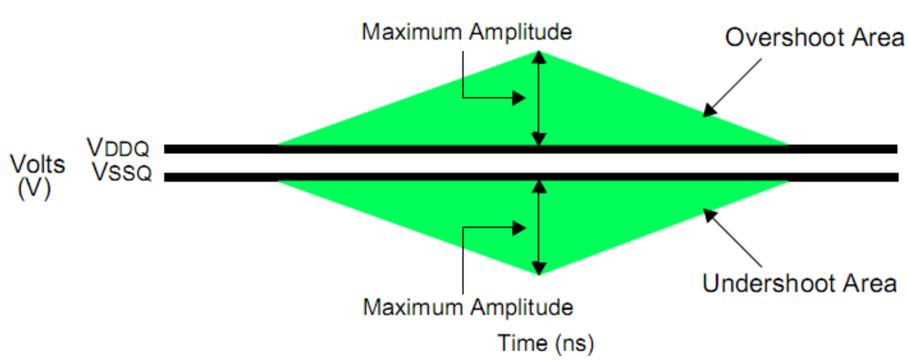


Figure 100 – Clock, Data, Strobe and Mask Overshoot and Undershoot Definition

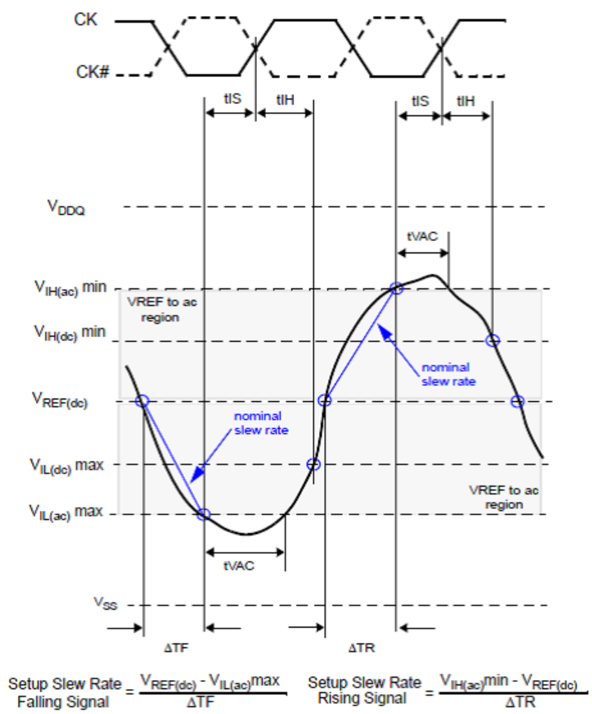


Figure 111 – Illustration of nominal slew rate and tVAC for setup time tIS(for ADD/CMD with respect to clock)

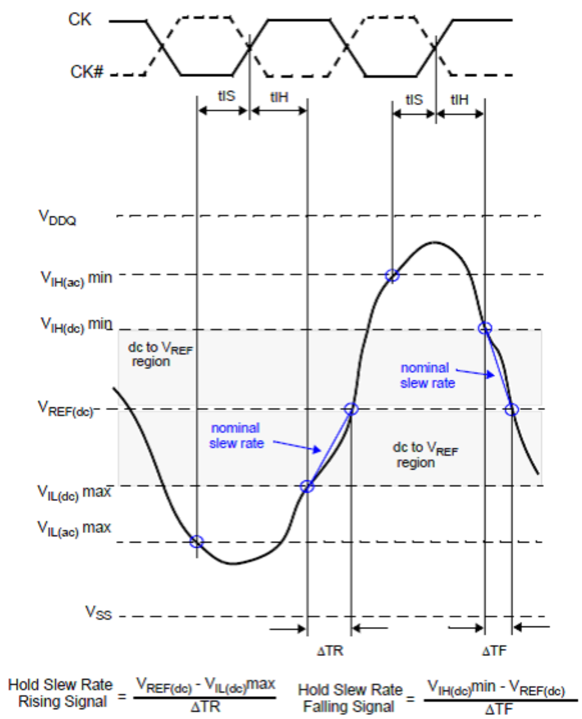


Figure 112 – Illustration of nominal slew rate for hold time tIS(for ADD/CMD with respect to clock)

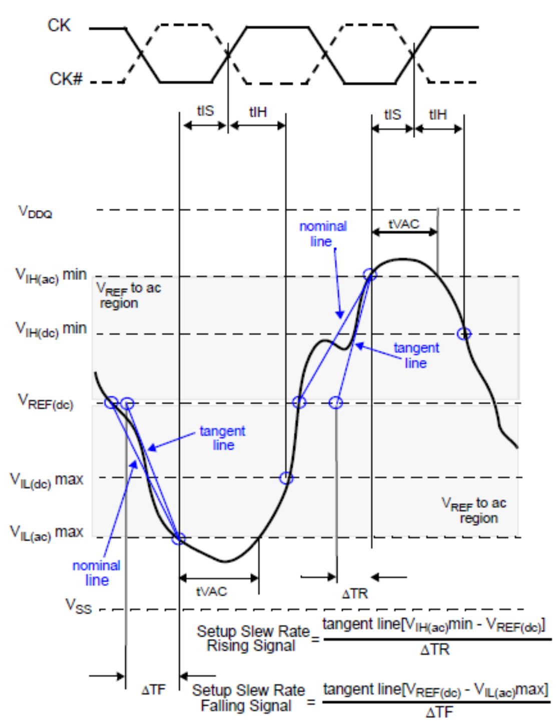


Figure 113 – Illustration of tangent line for setup time tIS(for ADD/CMD with respect to clock)

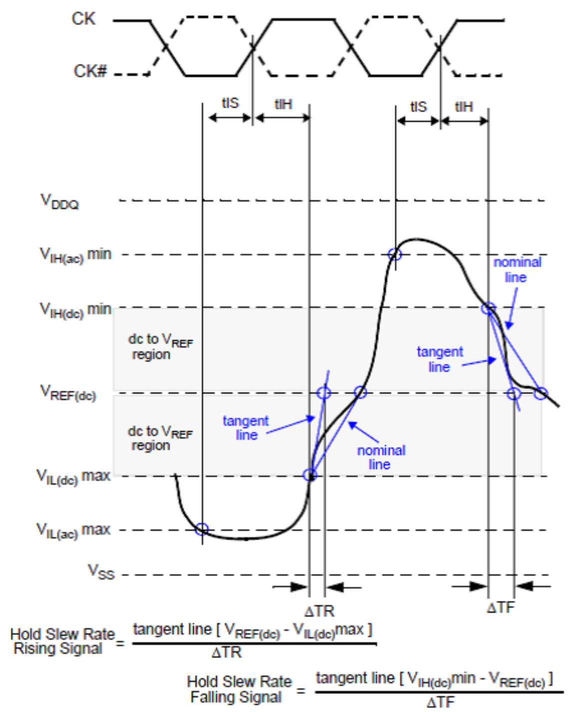


Figure 114 – Illustration of tangent line for hold time tIH(for ADD/CMD with respect to clock)

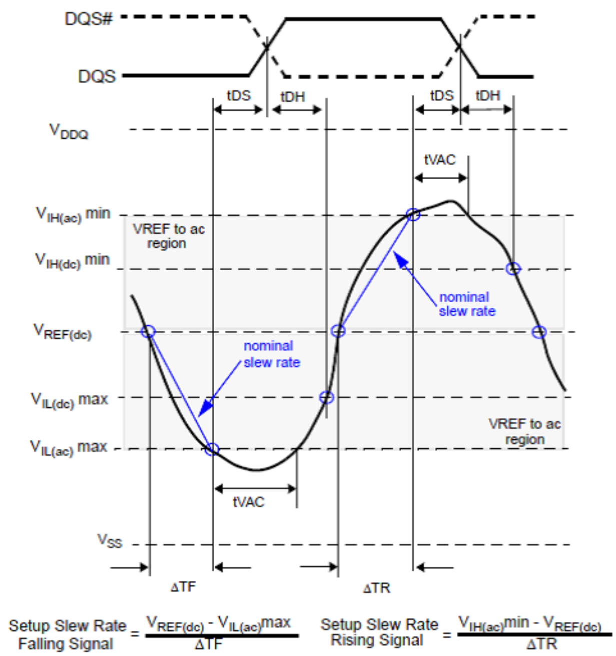


Figure 115 – Illustration of nominal slew rate and tVAC for setup time tDS(for DQ with respect to strobe)

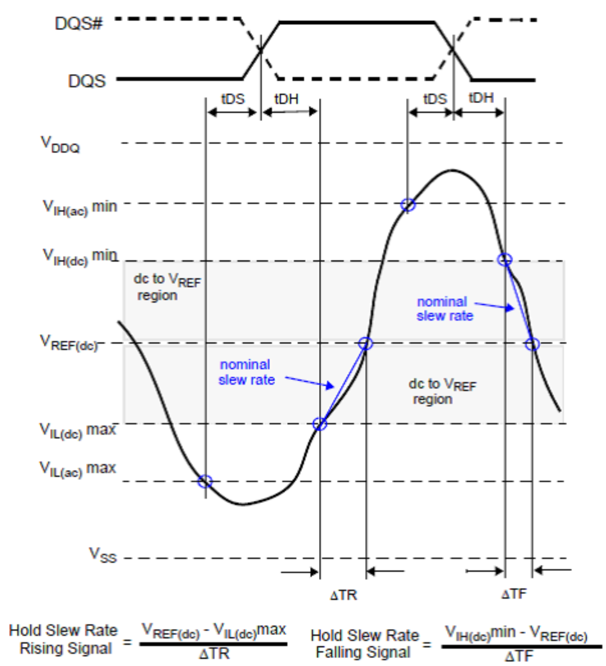


Figure 116 – Illustration of nominal slew rate for hold time tDH (for DQ with respect to strobe)

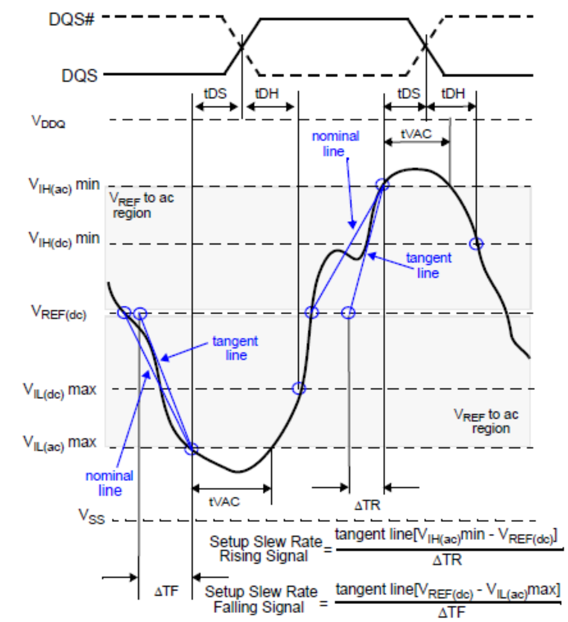


Figure 117 – Illustration of tangent line for setup time tDS (for DQ with respect to strobe)

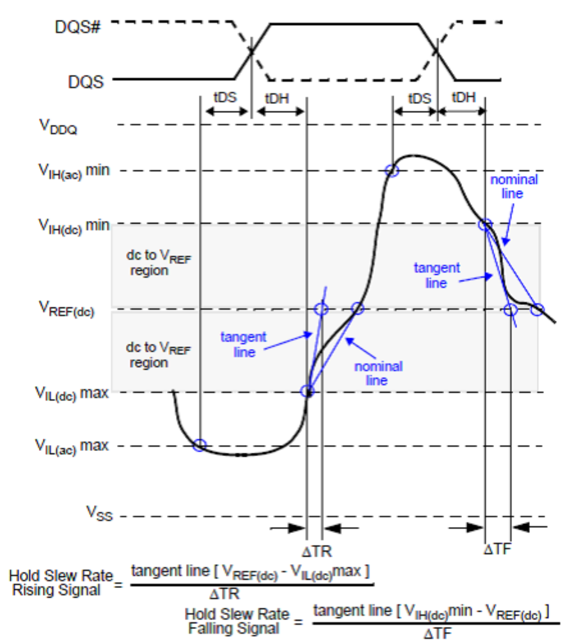
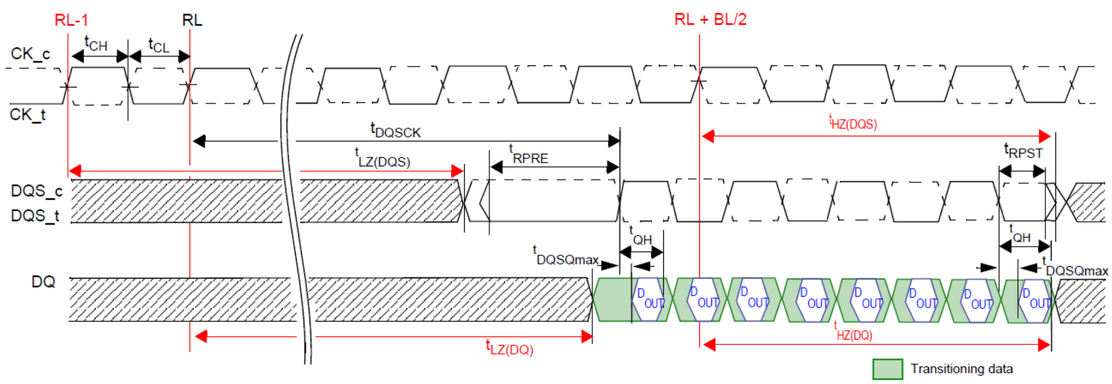


Figure 118 – Illustration of tangent line for hold time tDH (for DQ with respect to strobe)

Reference Figures from JESD209-4 Document



NOTE 1 tDQSCK can span multiple clock periods.
NOTE 2 An effective burst length of 8 is shown.

Figure 119 – Read Output Timing

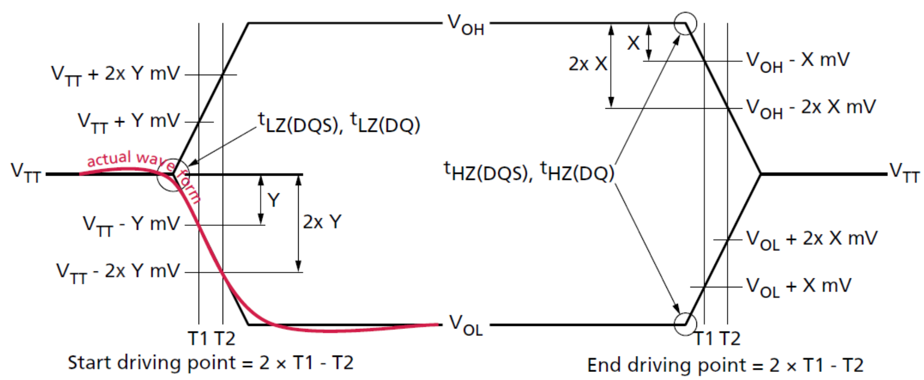


Figure120–tLZ and tHZ method for calculating transitions and endpoints

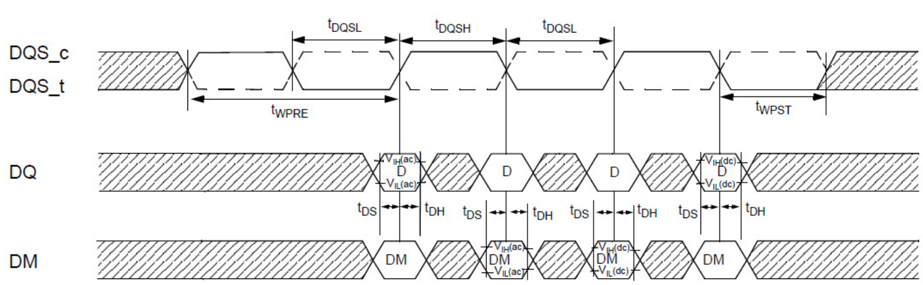


Figure121–Data input (write) timing

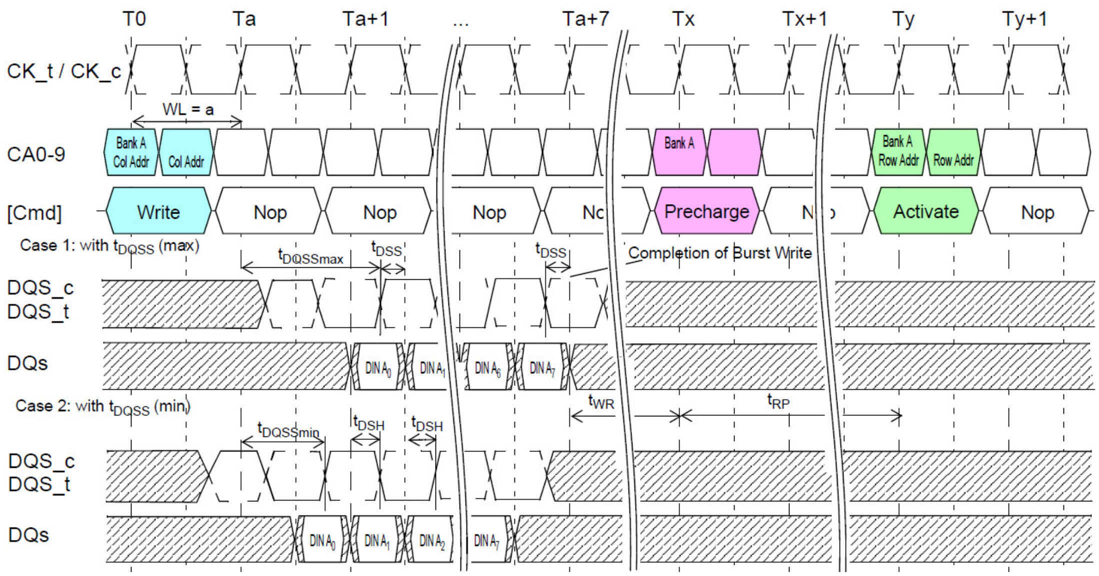


Figure122–LPDDR4Burst Write

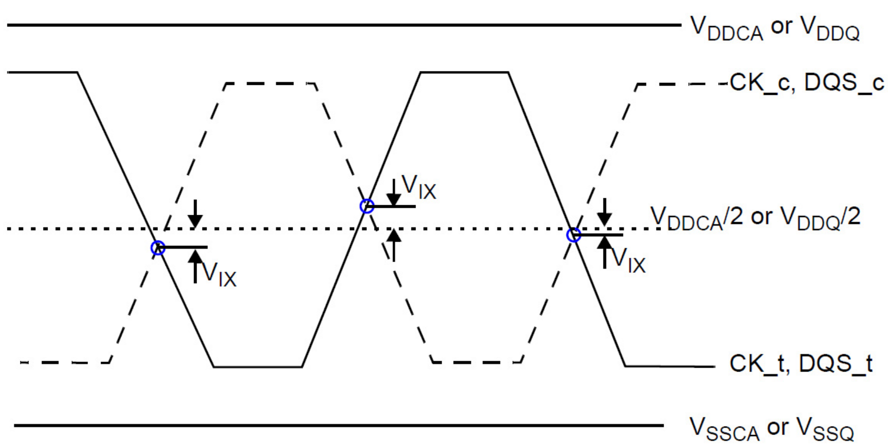


Figure 123 –Vix Definition

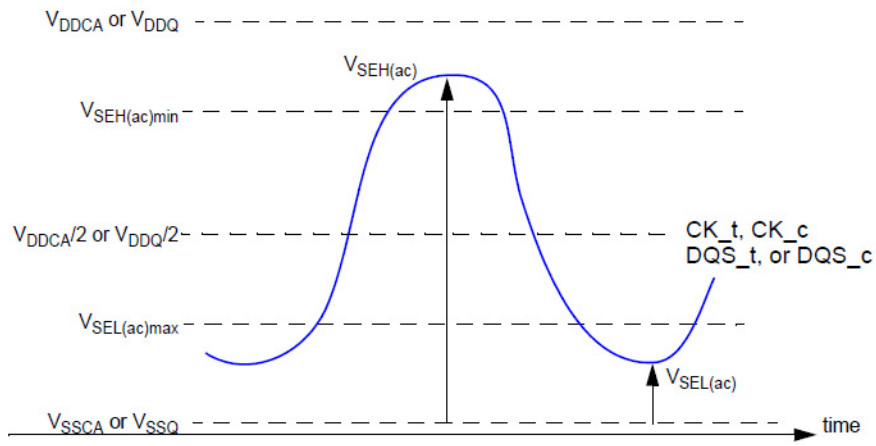


Figure 124 –Single-ended requirement for differential signals

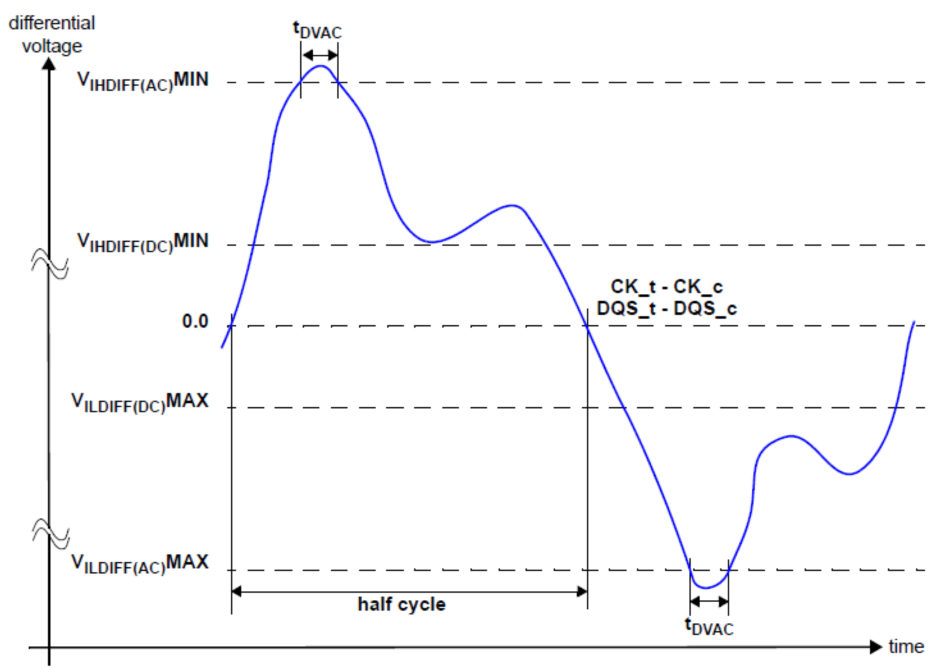


Figure125–Definition of differential ac-swing and "time above ac-level" tDVAC

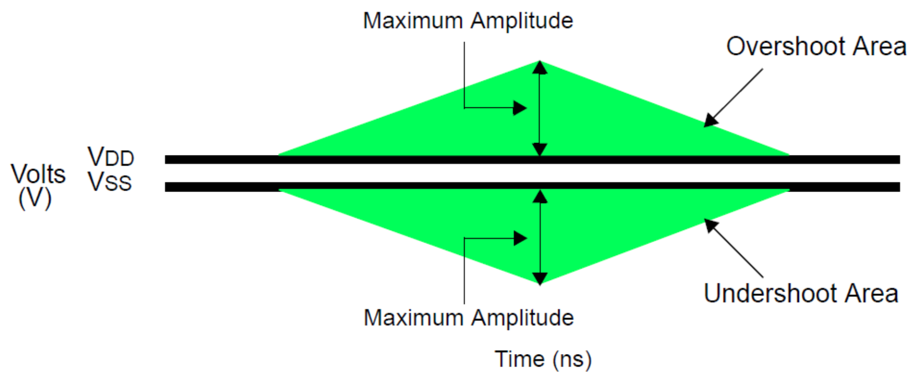


Figure 126 –Overshoot and Undershoot Definition

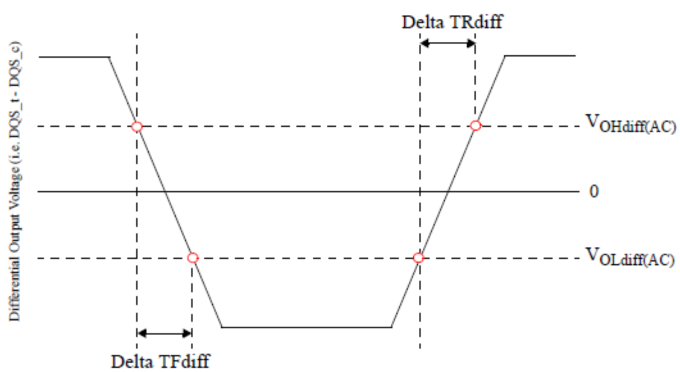


Figure127–Differential Output Slew Rate Definition

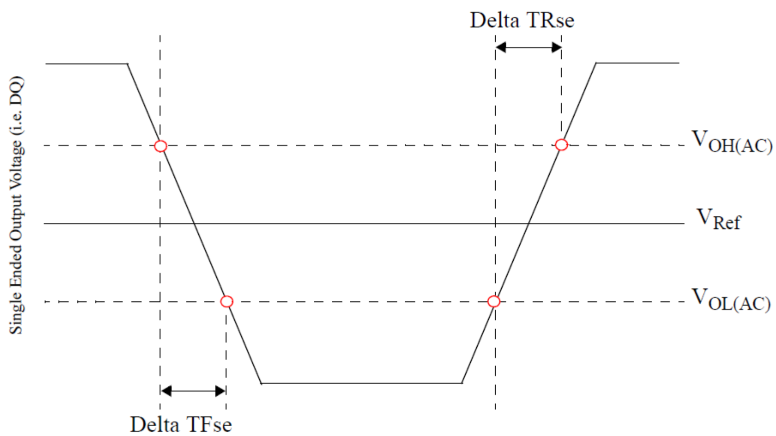


Figure 128 –Single Ended Output Slew Rate DefinitionDelta

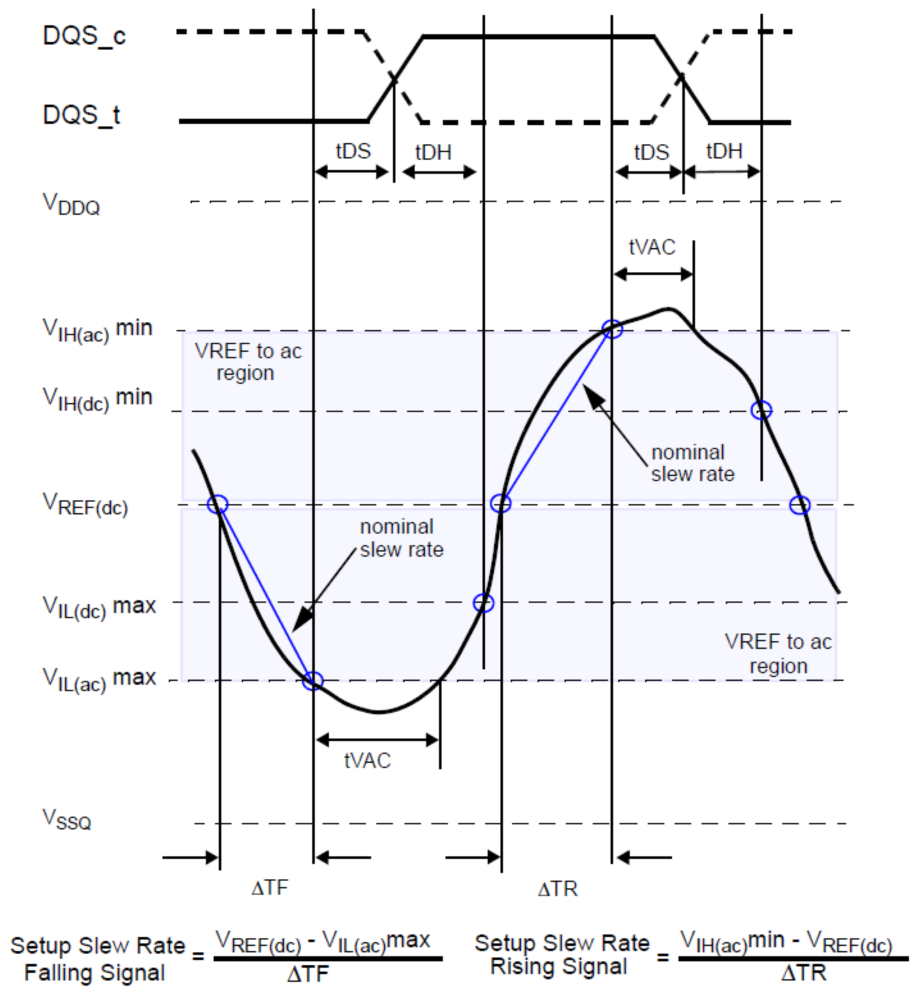


Figure129–Illustration of nominal slew rate and tVAC for setup time tDS for DQ with respect to strobe

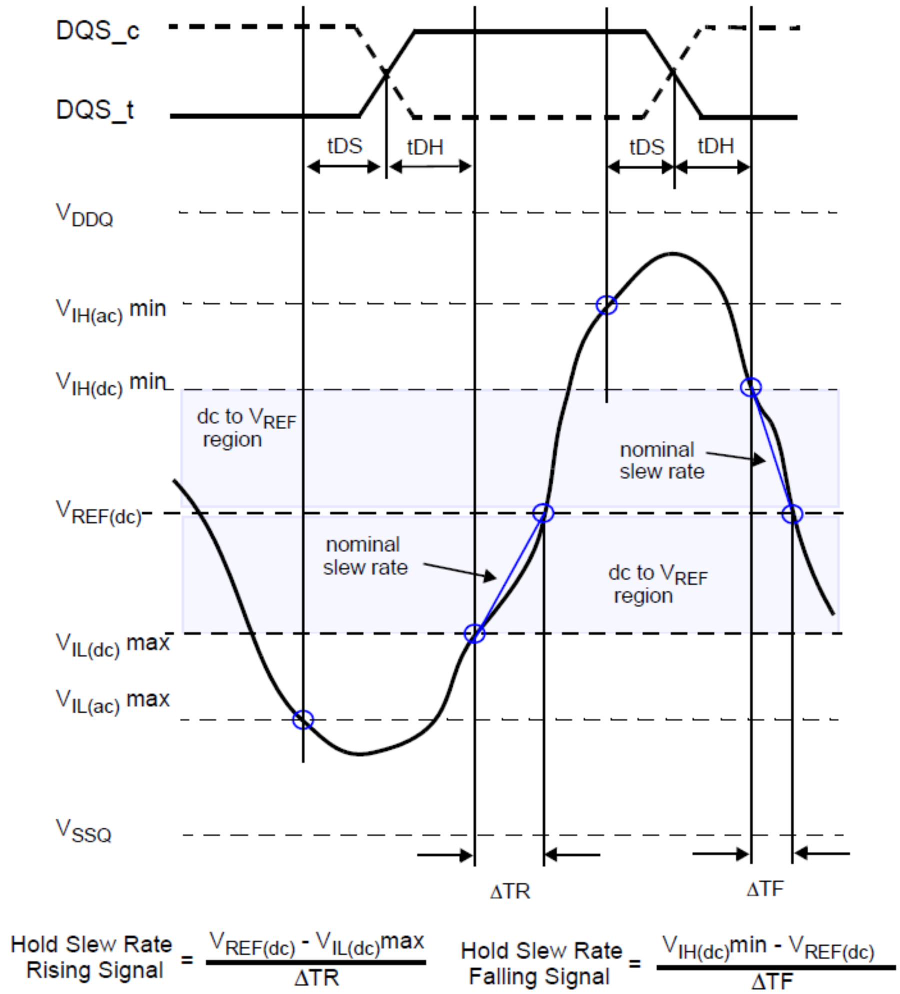


Figure 130 –Illustration of nominal slew rate for hold time tDH for DQ with respect to strobe

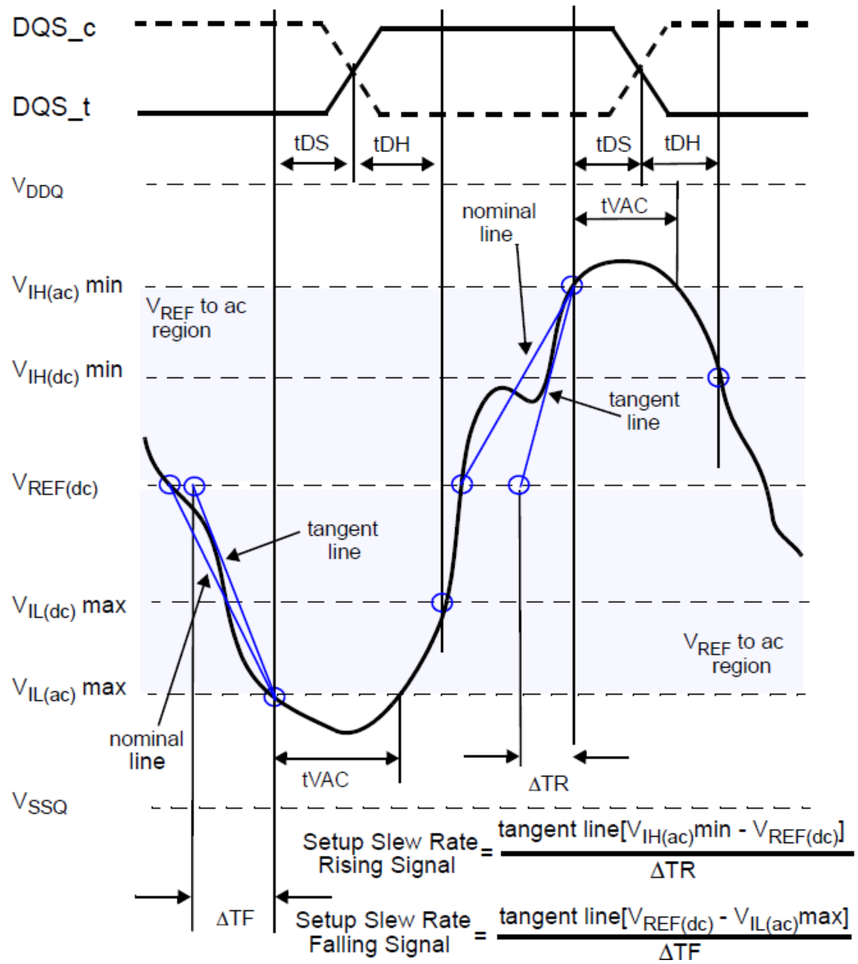


Figure 131 –Illustration of tangent line for setup time tDS for DQ with respect to strobe

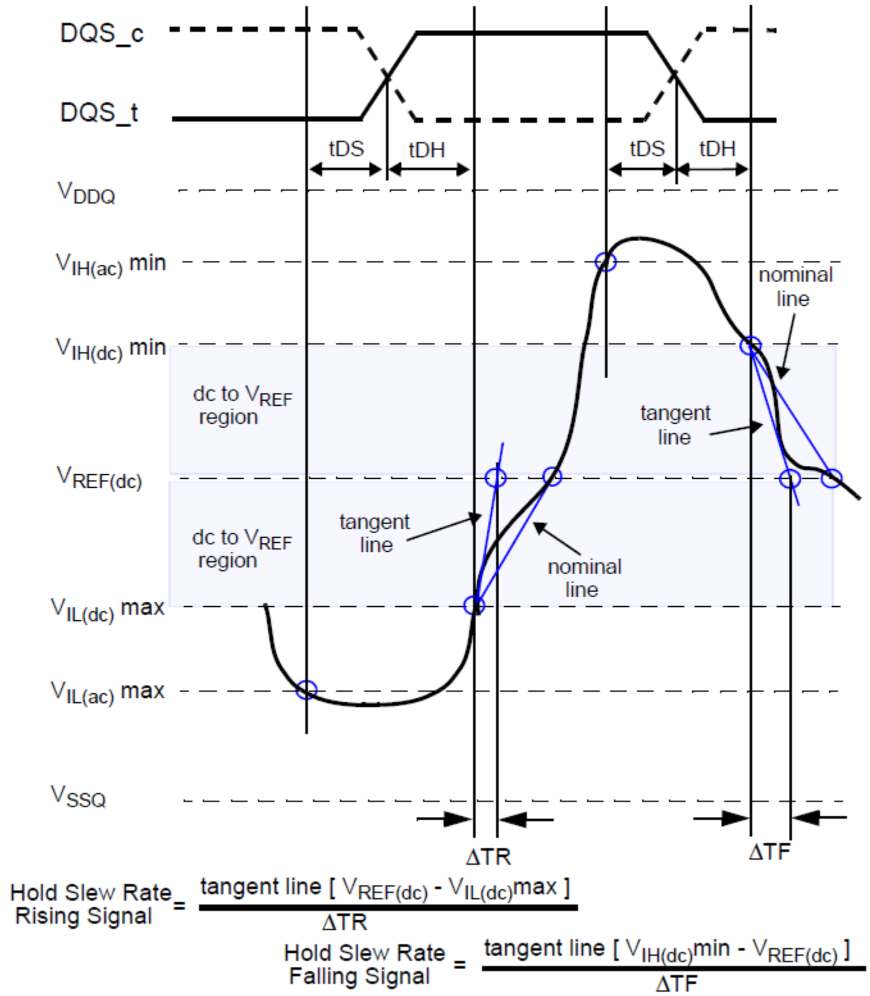


Figure 132 –Illustration of tangent line for for hold time tDH for DQ with respect to strobe

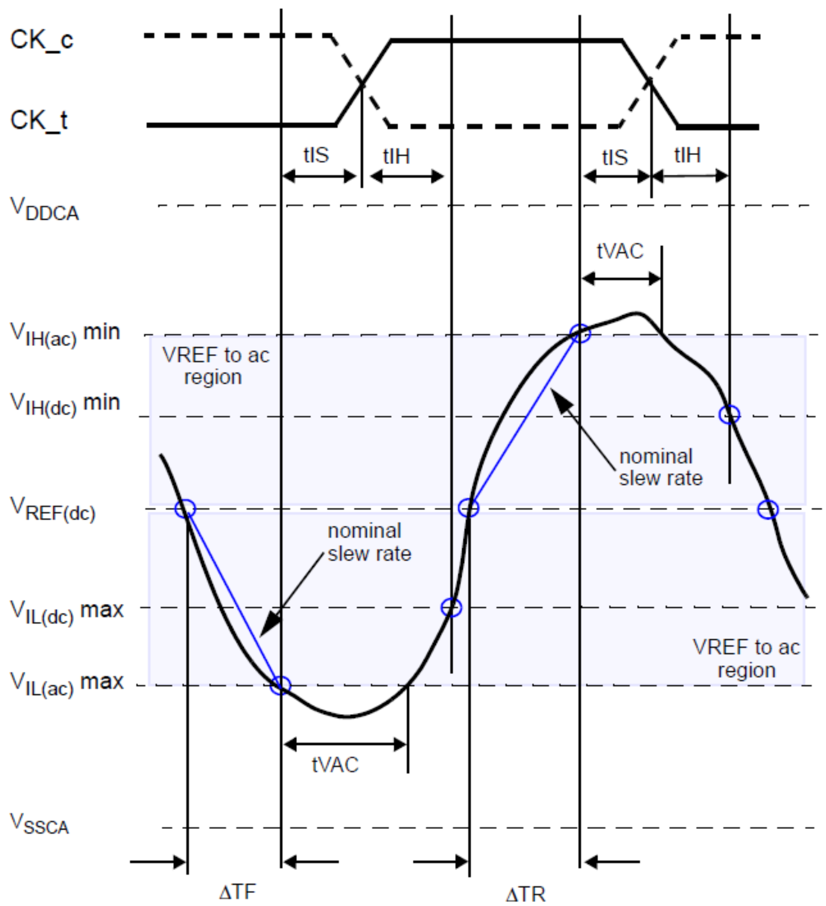


Figure133–Illustration of nominal slew rate and tVAC for setup time tIS for CA and CS_n with respect to clock

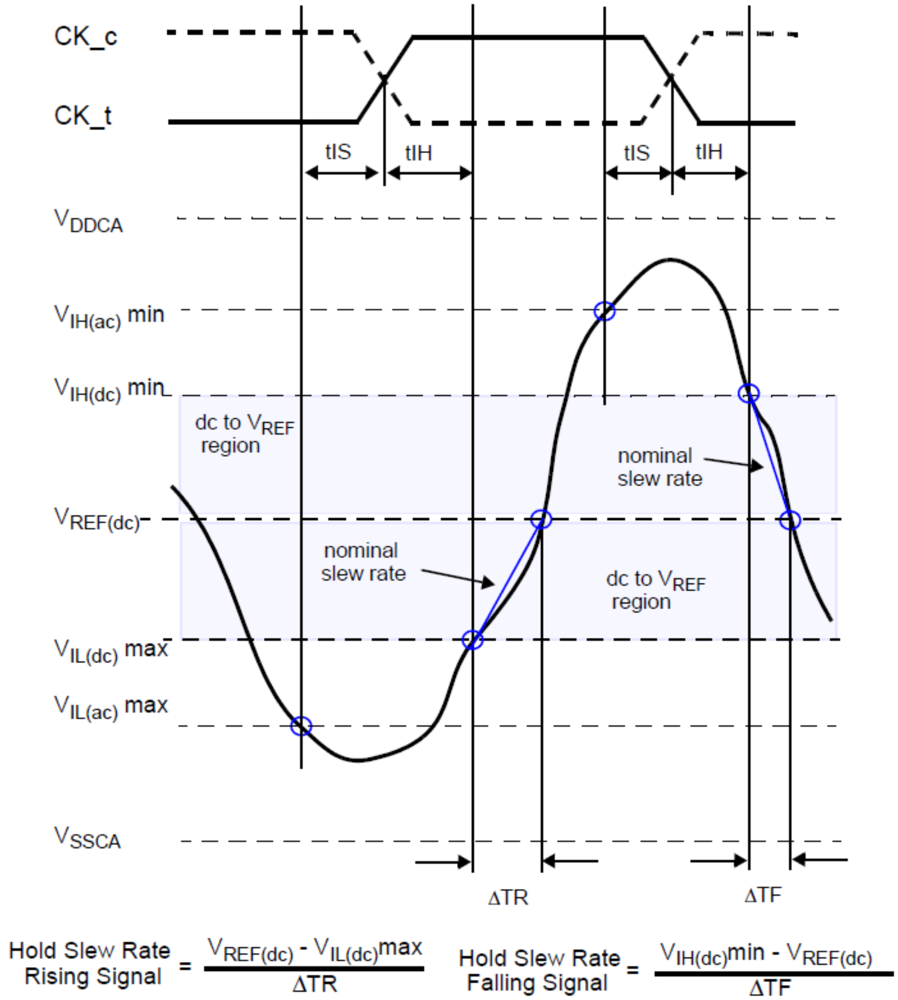


Figure134–Illustration of nominal slew rate for hold time tIH for CA and CS_n with respect to clock

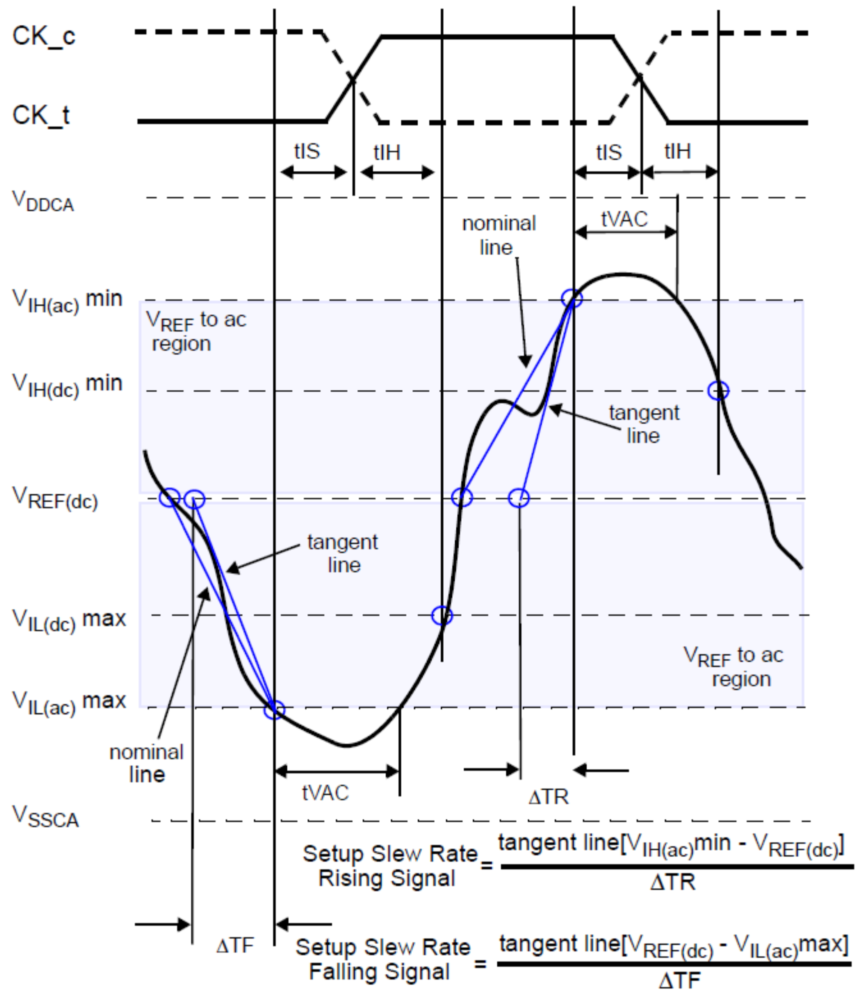


Figure 135 –Illustration of tangent line for setup time tIS for CA and CS_n with respect to clock

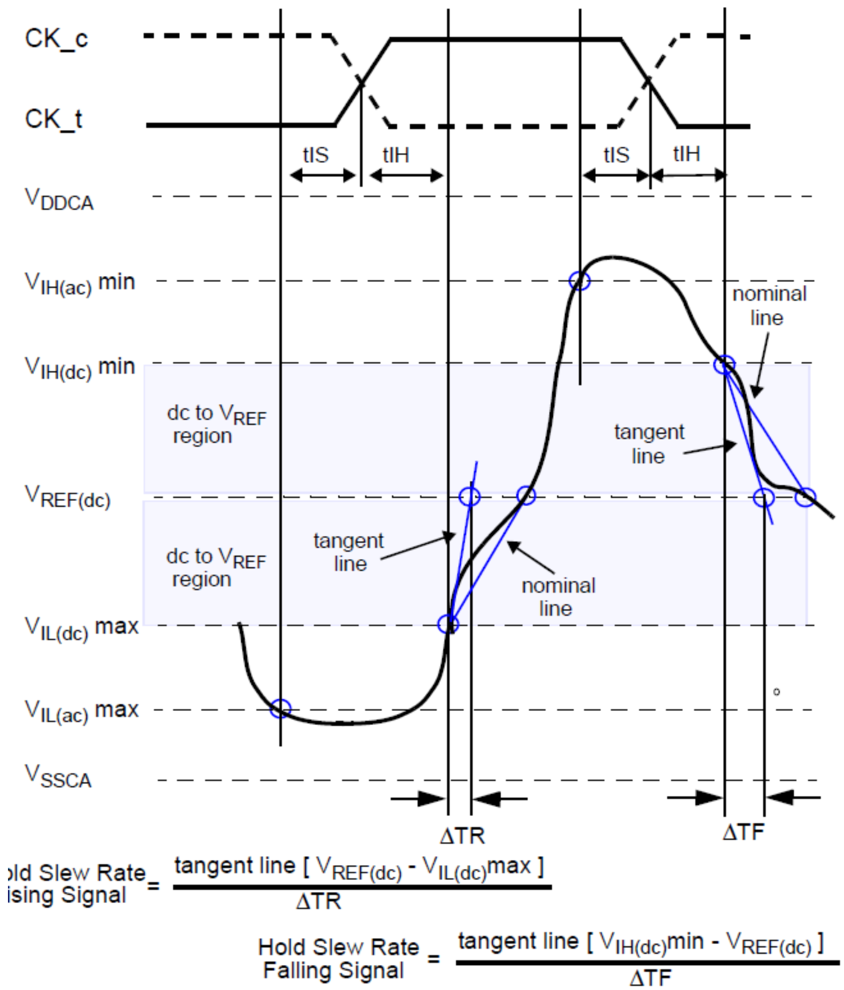


Figure136–Illustration of tangent line for for hold time tIH for CA and CS_n with respect to clock

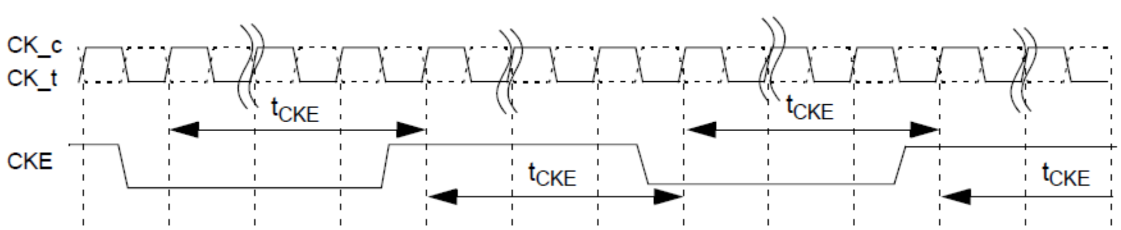


Figure 137 –CKE-Intensive Environment

B Calibrating the Infiniium Oscilloscope and Probe

This section describes the Keysight Infiniium digital storage oscilloscope calibration procedures.

Oscilloscope Internal Calibration

This will perform an internal diagnostic and calibration cycle for the oscilloscope. For the Keysight oscilloscope, this is referred to as Calibration.

Required Equipment for Oscilloscope Calibration

To calibrate the Infiniium oscilloscope in preparation for running the MOST automated tests, you need the following equipment:

- Keyboard, qty = 1, (provided with the Keysight Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Keysight Infiniium oscilloscope).
- Precision 3.5 mm BNC to SMA male adapter, Keysight p/n 54855-67604, qty = 2 (provided with the Keysight Infiniium oscilloscope).
- Calibration cable (provided with Keysight Infiniium oscilloscopes). Use a good quality 50 Ω BNC cable.

Running the Oscilloscope Internal Calibration

This Calibration will take about 50 minutes. Perform the following steps:

1. Set up the oscilloscope with the following steps:
   a. Connect the keyboard, mouse, and power cord to the rear of the oscilloscope.
   b. Plug in the power cord.
   c. Turn on the oscilloscope by pressing the power button located on the lower left of the front panel.
   d. Allow the oscilloscope to warm up at least 30 minutes prior to starting the calibration procedure in step 3 below.
2. Locate and prepare the accessories that will be required for the internal calibration:
   a. Locate the calibration cable.
   b. Locate the two Keysight precision SMA/BNC adapters.
   c. Attach one SMA adapter to the other end of the calibration cable - hand tighten snugly.
   d. Attach another SMA adapter to the other end of the calibration cable - hand tighten snugly.

3 Referring to the following figure, perform the following steps:

a Click the **Utilities > Calibration...** menu to open the Calibration dialog box.

Figure 5 Accessing the Calibration Menu

4 Referring to the following figure, perform the following steps to start the calibration:

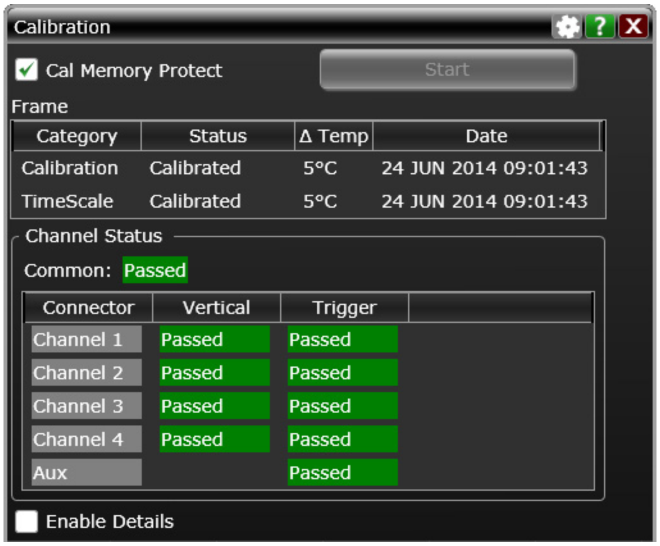


Figure 6 Oscilloscope Calibration Window

- **a** Uncheck the **Cal Memory Protect** checkbox.
- **b** Click the **Start** button to begin the calibration.
- **c** During the calibration of channel 1, if you are prompted to perform a **Time Scale Calibration**, as shown in the following figure, click the **Std+Dflt** button to continue the calibration, using the Factory default calibration factors.

  If you are prompted to choose a type of Time Scale Calibration, as shown in the following figure, choose the **Standard Cal and Default Time Scale** and click **Ok** to continue the calibration using the Factory default calibration factors.

Figure 7 Time Scale Calibration Dialog Box

- **d** When the calibration procedure is complete, you will be prompted with a Calibration Complete message window. Click the **OK** button to close this window.
- **e** Confirm that the Vertical and Trigger Calibration Status for all Channels passed.
- **f** Click the **Close** button to close the calibration window.
- **g** The internal calibration is completed.

NOTE

These steps do not need to be performed every time a test is run. However, if the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, this calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities > Calibration...** menu.

Probe Calibration

Before performing MOST tests, you should calibrate the probes. Calibration of the solder-in probe heads consist of a vertical calibration and a skew calibration. The vertical calibration should be performed before the skew calibration. Both calibrations should be performed for best probe measurement performance.

Required Equipment for Probe Calibration

The calibration procedure requires the following parts.

- BNC (male) to SMA (male) adapter.
- Deskew fixture.
- 50 Ω SMA terminator.

Connecting the Probe for Calibration

For the following procedure, refer to the following figure.

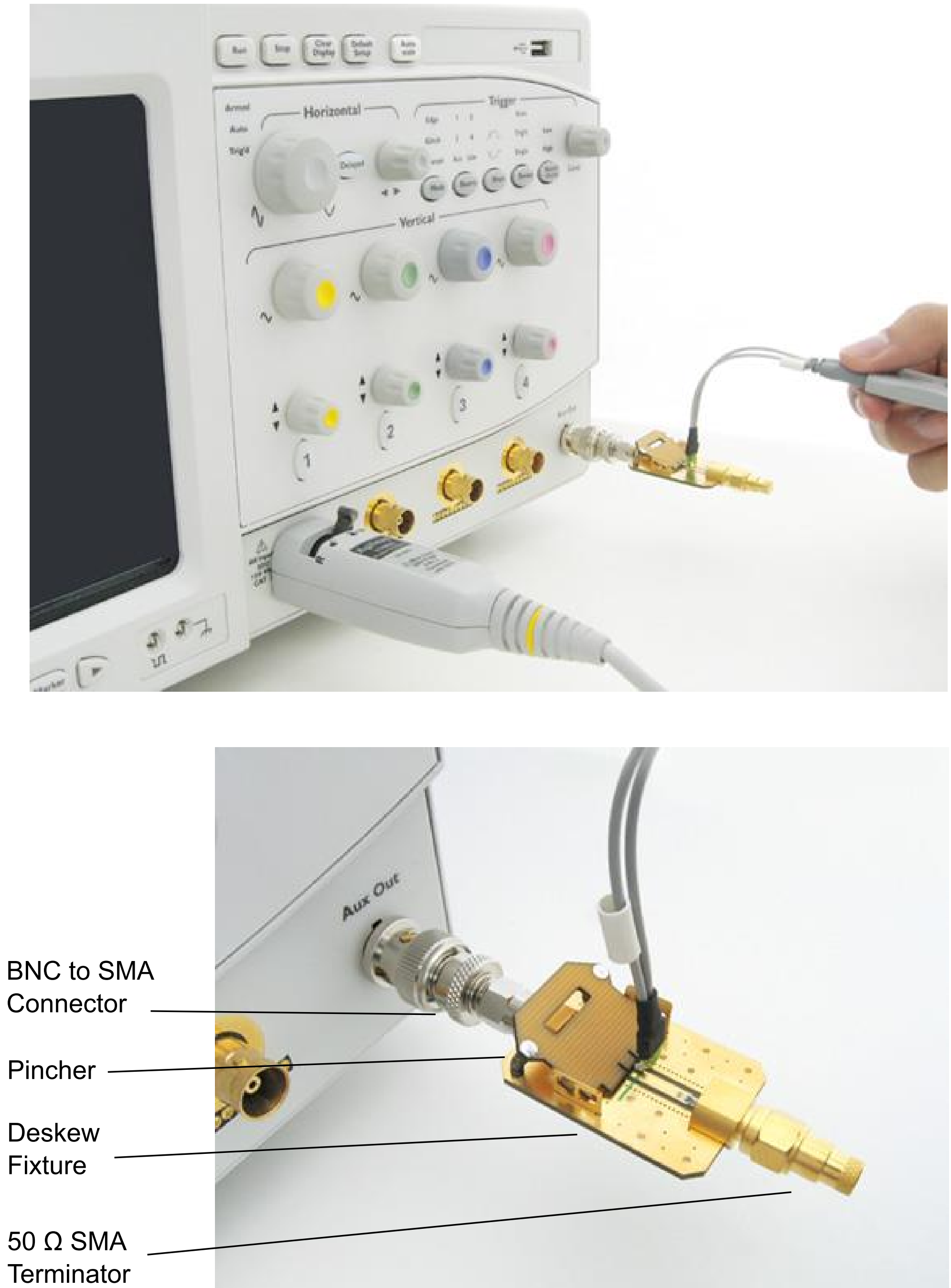


Figure 8 Solder-in Probe Head Calibration Connection Example

1. Connect BNC (male) to SMA (male) adapter to the deskew fixture on the connector closest to the yellow pincher.
2. Connect the 50 Ω SMA terminator to the connector farthest from yellow pincher.

3 Connect the BNC side of the deskew fixture to the Aux Out BNC of the Infiniium oscilloscope.

4 Connect the probe to an oscilloscope channel.

5 To minimize the wear and tear on the probe head, it should be placed on a support to relieve the strain on the probe head cables.

6 Push down the back side of the yellow pincher. Insert the probe head resistor lead underneath the center of the yellow pincher and over the center conductor of the deskew fixture. The negative probe head resistor lead or ground lead must be underneath the yellow pincher and over one of the outside copper conductors (ground) of the deskew fixture. Make sure that the probe head is approximately perpendicular to the deskew fixture.

7 Release the yellow pincher.

Verifying the Connection

1 On the Infiniium oscilloscope, press the **[Auto Scale]** key on the front panel.

2 Set the volts per division to **100 mV/div**.

3 Set the horizontal scale to **1.00 ns/div**.

4 Set the horizontal position to approximately **3 ns**. You should see a waveform similar to that in the following figure.

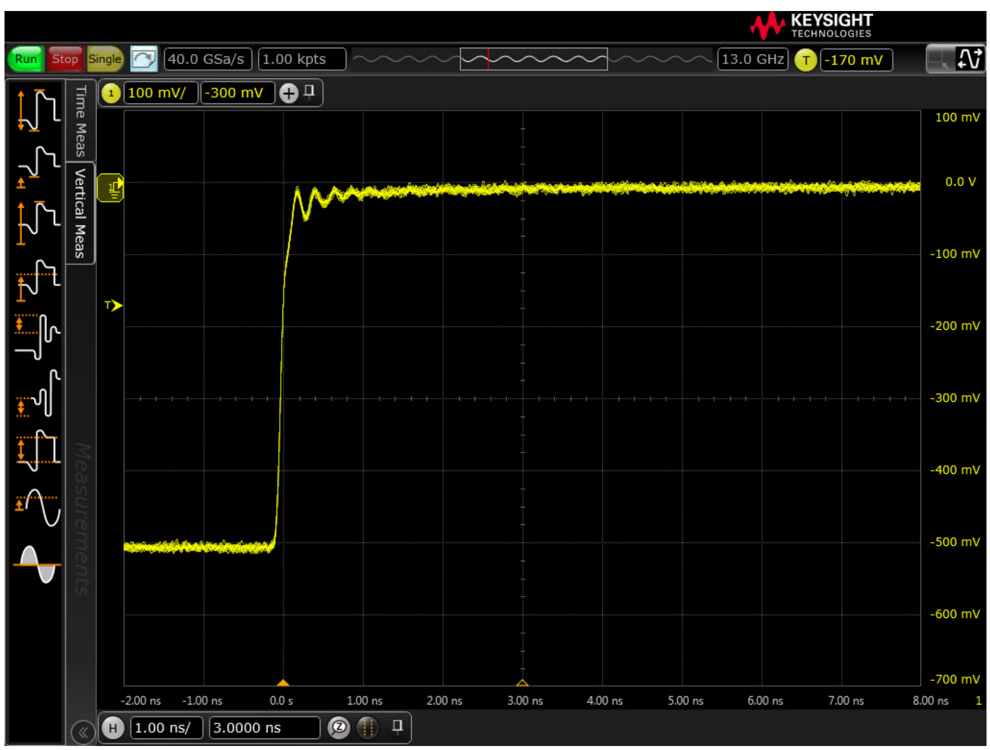


Figure 9 Good Connection Waveform Example

If you see a waveform similar to that of the following figure, then you have a bad connection and should check all of your probe connections.

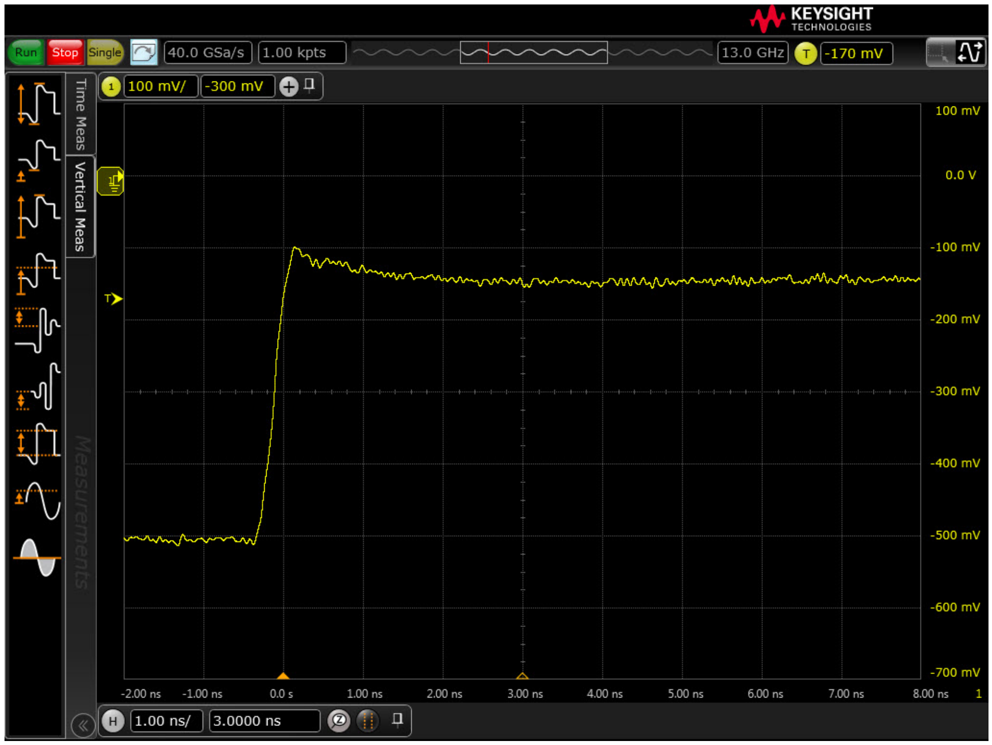


Figure 10 Bad Connection Waveform Example

Running the Probe Calibration and Deskew

1 On the Infiniium oscilloscope in the **Setup** menu, select the channel connected to the probe, as shown in the following figure.

Figure 11 Channel Setup Window

2 In the Channel Setup dialog box, select the **Probe Cal...** button, as shown in the following figure.

Figure 12 Channel Dialog Box

3 In the Probe Calibration dialog box, select the **Calibrated Atten** radio button.

4 Select the **Start Atten/Offset Cal...** button and follow the on-screen instructions for vertical calibration procedure.

Figure 13 Probe Calibration Window

5 Once the vertical calibration has successfully completed, select the **Calibrated Skew...** button.

6 Select the **Start Skew Calibration...** button and follow the on-screen instructions for the skew calibration.

At the end of each calibration, the oscilloscope will prompt you if the calibration was or was not successful.

Verifying the Probe Calibration

If you have successfully calibrated the probe, it is not necessary to perform this verification. However, if you want to verify that the probe was properly calibrated, the following procedure will help you verify the calibration.

The calibration procedure requires the following parts:

- BNC (male) to SMA (male) adapter.
- SMA (male) to BNC (female) adapter.
- BNC (male) to BNC (male) 12 inch cable such as the Keysight 8120-1838.
- Keysight 54855-61620 calibration cable (Infiniium oscilloscopes with bandwidths of 6 GHz and greater only).
- Keysight 54855-67604 precision 3.5 mm adapters (Infiniium oscilloscopes with bandwidths of 6 GHz and greater only).
- Deskew fixture.

For the following procedure, refer to the following figure.

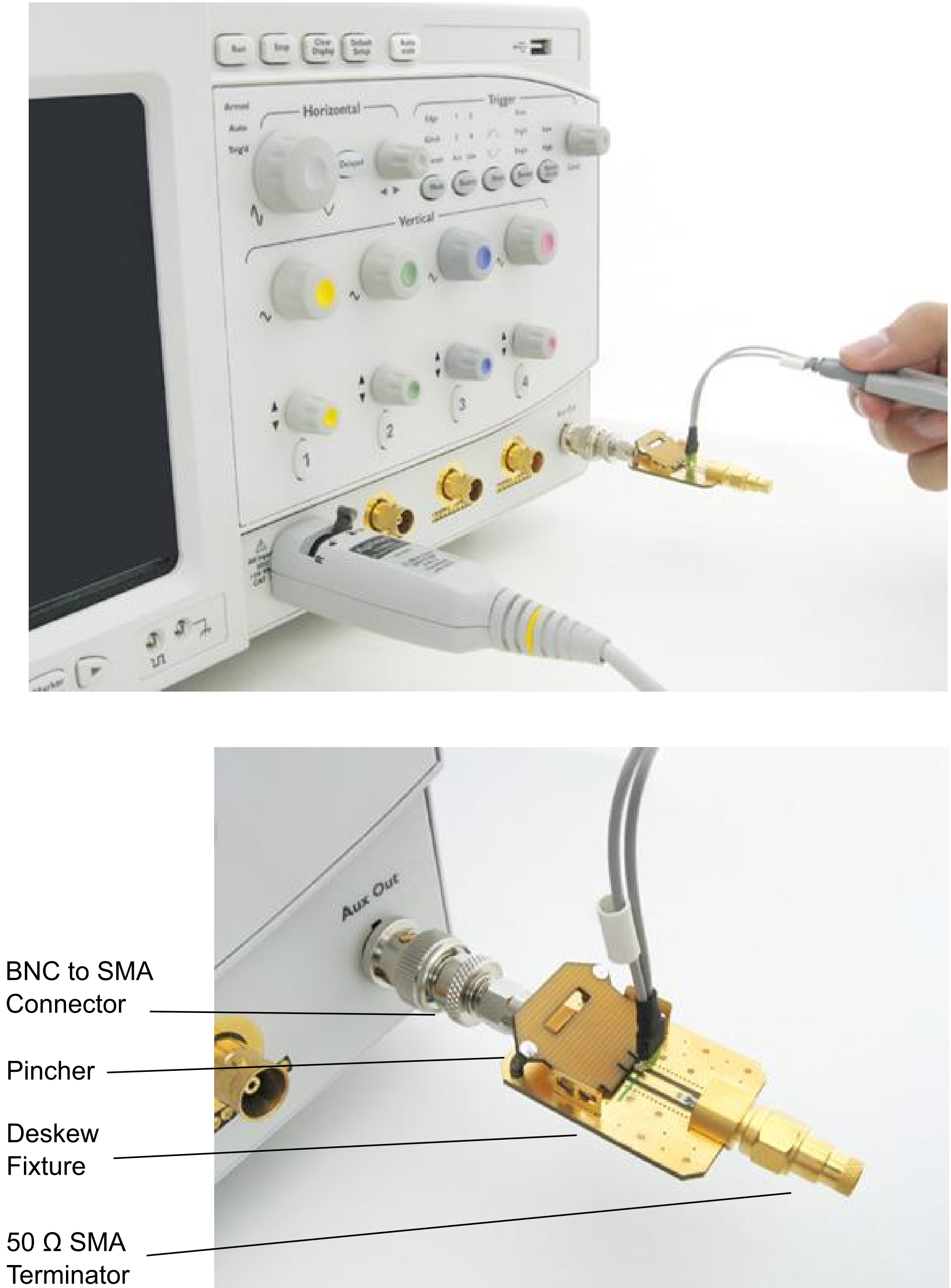


Figure 14 Probe Calibration Verification Connection Example

1 Connect BNC (male) to SMA (male) adapter to the deskew fixture on the connector closest to the yellow pincher.

2 Connect the SMA (male) to BNC (female) to the connector farthest from the yellow pincher.

3 Connect the BNC (male) to BNC (male) cable to the BNC connector on the deskew fixture to one of the unused oscilloscope channels. For infiniium oscilloscopes with bandwidths of 6 GHz and greater, use the 54855-61620 calibration cable and the two 54855-64604 precision 3.5 mm adapters.
4 Connect the BNC side of the deskew fixture to the Aux Out BNC of the Infiniium oscilloscope.
5 Connect the probe to an oscilloscope channel.
6 To minimize the wear and tear on the probe head, it should be placed on a support to relieve the strain on the probe head cables.
7 Push down on the back side of the yellow pincher. Insert the probe head resistor lead underneath the center of the yellow pincher and over the center conductor of the deskew fixture. The negative probe head resistor lead or ground lead must be underneath the yellow pincher and over one of the outside copper conductors (ground) of the deskew fixture. Make sure that the probe head is approximately perpendicular to the deskew fixture.
8 Release the yellow pincher.
9 On the oscilloscope, press the autoscale button on the front panel.
10 Select Setup menu and choose the channel connected to the BNC cable from the pull-down menu.
11 Select the **Probes...** button.
12 Select the **Configure Probe System** button.
13 Select **User Defined Probe** from the pull-down menu.
14 Select the **Calibrate Probe...** button.
15 Select the **Calibrated Skew** radio button.
16 Once the skew calibration is completed, close all dialog boxes.
17 Select the **Start Skew Calibration...** button and follow the on-screen instructions.
18 Set the vertical scale for the displayed channels to **100 mV/div**.
19 Set the horizontal range to **1.00 ns/div**.
20 Set the horizontal position to approximately **3 ns**.
21 Change the vertical position knobs of both channels until the waveforms overlap each other.
22 Select the Setup menu choose **Acquisition...** from the pull-down menu.
23 In the Acquisition Setup dialog box enable averaging. When you close the dialog box, you should see waveforms similar to that in the following figure.

Figure 15 Calibration Probe Waveform Example

NOTE

Each probe is calibrated with the oscilloscope channel to which it is connected. Do not switch probes between channels or other oscilloscopes, or it will be necessary to calibrate them again. It is recommended that the probes be labeled with the channel on which they were calibrated.

Index

U

V

W